Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Features

- Up to 3,000,000 usable NAND2 equivalent gates using standard cell architecture
- Toggle rates up to 1.2 GHz
- Advanced 0.25µ bulk silicon gate CMOS processed in a commercial fab
- Operating voltage of 100% 3.3V or 3.3V I/O and 2.5V core
- Input buffers are 5-volt tolerant
- Multiple product assurance levels available, QML V and Q, military, industrial
- Radiation hardened from 100 krad(Si) to 1 Mrad total dose available using CAES RadHard techniques
- SEU-immune to less than 1.0E-10 errors/bits-day available using special library cells
- Robust CAES Design Library of cells and macros
- Support for Verilog and VHDL design languages on Linux workstations
- Cell models validated in Mentor Graphics® and Synopsys™ design environments
- Full complement of industry standard IP cores
- Various RAM configurations available
- Supports cold sparing for power down applications
- Power dissipation of 0.04µW/MHz/gate at V_{DDCORE} 2.5V and 20% duty cycle and 0.06µW/MHz/gate at V_{DDCORE} 3.3V and 20% duty cycle
- External chip capacitor attachment option available to space quality levels (for improved SSO response)

Product Description

CAES high-performance UT0.25µ Hardened-by-Design ASIC standard cell family features densities up to 3,000,000 NAND2 equivalent gates and is available in multiple quality assurance levels such as MIL-PRF-38535, QML V and Q, military, industrial grades, and non-RadHard versions.

For those designs requiring stringent radiation hardness, CAES 0.25µ process employs a special technique that enhances the total dose radiation hardness from 100 krad(Si) to 1 Mrad while maintaining circuit density and reliability. In addition, for greater transient radiation hardness and latch-up immunity, the deep sub-micron process is built on epitaxial wafers.

Developed from CAES patented architectures, the 0.25 ASIC family uses a highly efficient standard cell architecture for internal cell instantiation. Combined with state-of-the-art, timing driven placement and routing tools, the area utilization and signal routing of transistors is maximized using five levels of metal interconnect.

The UT0.25µ HBD ASIC family is supported by an extensive cell library that includes SSI, MSI, and 54XX equivalent functions, as well as PLL, RAM, and cores. CAES core library includes the following functions:

- Intel 80C31® equivalent
- Intel 80C196® equivalent
- MIL-STD-1553 functions (BRCTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- RISC microcontroller
- Select RAM configurations (with optional MBIST and EDAC)
- Phase Locked Loop (PLL)
- CAES

We offer CAES LEON3 and RTL based IP.

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Table 1. Gate Densities

Die Size (Mils estimate)	Equivalent Usable Gates [1]	Signal I/O [2]	Power & Ground PADS
245	276,890	160	48
313	501,760	216	64
374	757,350	265	79
426	1,024,000	308	92
510	1,524,122	376	112
578	2,007,040	431	129
642	2,524,058	484	144
699	3,029,402	530	158

Notes:

1) Based on NAND2 equivalents plus 20% routing overhead. Actual usable gate count is design-dependent.

Low-noise Device and Package Solutions

Separate on-chip power and ground buses are provided for internal cells and output drivers which further isolate internal design circuitry from switching noise.

In addition, CAES offers advanced low-noise package technology with multi-layer, co-fired ceramic construction featuring builtin isolated power and ground planes (see Table 2). These planes provide lower overall resistance/inductance through power and ground paths which minimize voltage drops during periods of heavy switching. These isolated planes also help sustain supply voltage during dose rate events, thus preventing rail span collapse.

Flatpacks are available with up to 352 leads; PGAs are available with up to 299 pins and LGAs/CCGAs to 624 pins. CAES flatpacks feature a non-conductive tie bar that helps maintain lead integrity through test and handling operations. In addition to the packages listed in Table 2, CAES offers custom package development and package tooling modification services for individual requirements.

Table 2. Packages

Type	Package
Flatpack	68, 84, 132, 172, 196, 208, 240, 256, 304, 352
PGA	299
LGA[4]	472, 624

Notes:

1) Contact CAES for specific package drawings.

2) External chip capacitor attachment option available to space quality levels (for improved SSO response).

3) CAES supports all JEDEC outline package designs. Listed packages are tooled.

4) LGA package formats can be provided with Solder Columns.

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Extensive Cell Library

The UT0.25µHBD standard cell family is supported by an extensive cell library that includes SSI, MSI, and 54XX-equivalent functions, as well as RAM and other library functions. User-selectable options for cell configurations include scan and radiation hardness (SEU) levels for all register elements, as well as output drive strength. Phase-Locked Loop (PLL) macro cells are derived from the CAES Standard Products UT7R995 RadClock™. They are available in three frequency ranges - 24MHz to 50MHz, 48MHz to 100MHz, and 96MHz to 200MHz. All PLLs support a power-down mode and phase lock indicator.

Refer to CAES UT0.25µHBD Design Manual for complete cell listing and details.

I/O Buffers

The UT0.25µHBD gate array family offers up to 530 signal I/O locations (note: device signal I/O availability is affected by package selection and pinout). The I/O cells can be configured by the user to serve as input, output, bidirectional, three-state, or additional power and ground pads. Output drive options range from 4 to 24mA. To drive larger off-chip loads, output drivers may be combined in parallel to provide additional drive up to 48mA.

Other I/O buffer features and options include:
- Pull-up and pull-down resistors
- Schmitt trigger
- LVDS
- PCI
- SSTL
- CML
- Cold Sparing

LVDS transmitter (Tx) and receiver (Rx) buffers are based on the CAES Standard Products UT54LVDS031LV LVDS driver and UT54LVDS032LV receiver products. They provide the same >400Mbps (200MHz) switching rates, 340mV nominal differential signaling levels, cold-sparing, transmitter enable, and receiver fail-safe circuitry. Each supports a power-down mode, putting the I/O buffers into their lowest power state. A unique CAES reference circuit improves performance matching between multiple Tx buffers and multiple Rx buffers.

The PCI I/O buffer is usable as an input, output or bidirect and is compliant to the PCI 2.2 specification.

CAES ASIC SSTL bidirect, tristate, and input buffers are based on the JESD8-15A standard for Stub Series Terminated Logic for 1.8V (SSTL_18) Class-1 and -2. They provide switching rates >200Mbps (100MHz) and all support a power-down mode.

JTAG Boundary-Scan

The UT0.25µ HBD arrays provide for a test access port and boundary-scan that conforms to the IEEE Standard 1149.1 (JTAG). Some of the benefits of this capability are:
- Easy test of complex assembled printed circuit boards
- Gain access to and control of internal scan paths
- Initiation of Built-In Self Test

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Clock Driver Distribution

CAES design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

Speed and Performance

CAES specializes in high-performance circuits designed to operate in harsh military and radiation environments. Table 3 presents a sampling of typical cell delays.

Note that the propagation delay for a CMOS device is a function of its fanout loading, input slew, supply voltage, operating temperature, and processing radiation tolerance. In a radiation environment, additional performance variances must be considered.

The UT0.25µHBD array family simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

Power Dissipation

Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. Radiation-tolerant processes exhibit power dissipation that is typical of CMOS processes. For a rigorous power estimating methodology, refer to the CAES UT0.25µHBD Design Manual or consult with a CAES Applications Engineer.

Typical Power Dissipation

0.04µW/Gate-MHz@2.5V	20% duty cycle
0.06µW/Gate-MHz@3.3V	20% duty cycle

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Table 3. Typical Cell Delays

Cell	Output Transition	Propagation Delay [1]	Propagation Delay [1]
Internal Gates		V_{DD} = 2.5V	V_{DD} = 3.3V
INV1, Inverter	HL	.123	.150
	LH	.155	.230
INV4, Inverter 4X	HL	.077	.104
	LH	.110	.179
NAND2, 2-Input NAND	HL	.159	.190
	LH	.186	.254
NOR2, 2-Input NOR	HL	.146	.171
	LH	.224	.303
DFF - CLK to Q	HL	.474	.647
	LH	.475	.613
LDL - CLK to Q	HL	.579	.766
	LH	.457	.671
Output Buffers			
OC33 {25,33} N4_C	HL	4.649	4.155
	LH	6.711	5.793
OC33 {25,33} N12_C	HL	3.125	2.937
	LH	3.875	3.519
Input Buffers			
IC33 {25,33} C	HL	.673	.573
	LH	.474	.667

Note:

1) All specifications in ns (typical). Output load capacitance is 50pF. Fanout loading for input buffers and gates is the equivalent of two gate input loads. For core cells and output buffers input slew is ~.2ns. For input buffer, input slew is 0.4ns (slew is measured from 30% - 70% of V_{DD}).
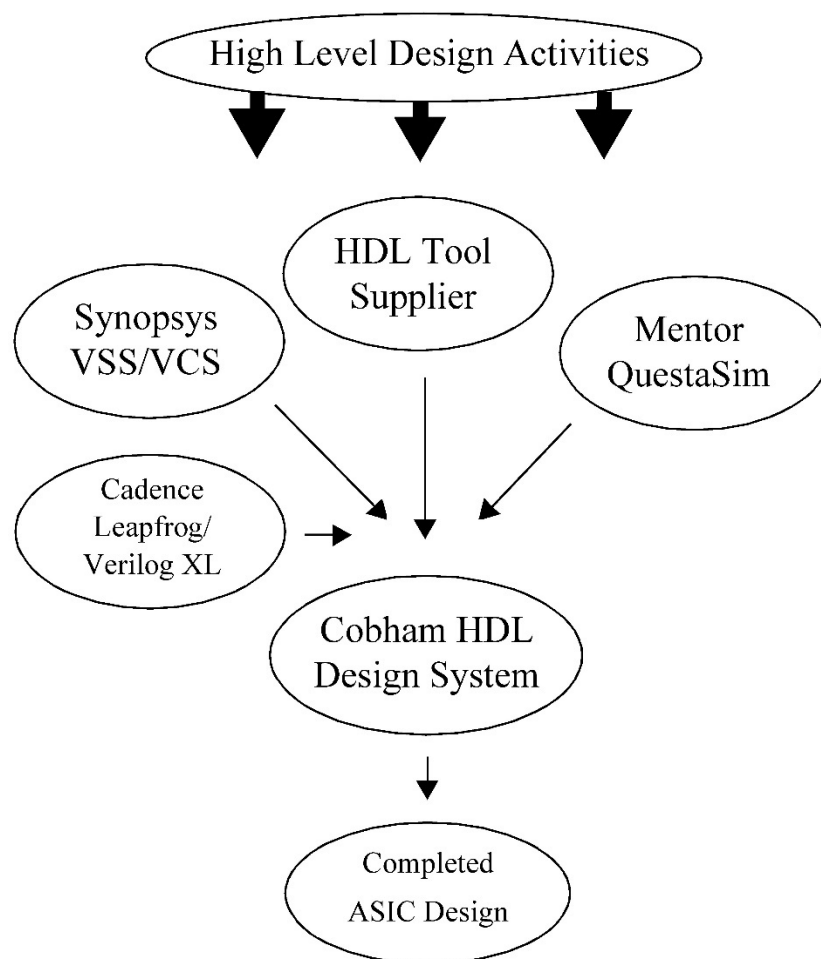
ASIC Design Software

Using a combination of state-of-the-art third-party and proprietary design tools, CAES delivers the CAE support and capability to handle complex, high-performance ASIC designs from design concept through design verification and test.

CAES flexible circuit creation methodology supports high level design methodology by providing synthesis libraries in Liberty syntax. Compiled technology files are provided for Synopsys synthesis and design analysis tools. Design verification is performed in any VHDL or Verilog simulation environment, using CAES robust libraries. CAES also supports Automatic Test Program Generation to improve design testing.

CAES HDL Design Systems

CAES offers a Hardware Description Language (HDL) design system supporting VHDL and Verilog. Both the VHDL and Verilog libraries provide sign-off quality models and robust tools.

CAES PIONEERING ADVANCED ELECTRONICS

4350 Centennial Blvd. | Colorado Springs CO 80907 USA | 1-800-645-8862 | cobhamaes.com

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

CAES Springs HDL Design Flow

The VHDL libraries are VITAL 3.0 compliant, and the Verilog libraries are OVI 1.0 compliant. With the library capabilities CAES provides, you can use High Level Design methods to synthesize your design for simulation. CAES also provides tools to verify that your HDL design will result in working ASIC devices.

Advantages of the CAES HDL Design Systems

- The CAES HDL Design System gives you the freedom to use tools from Synopsys, Mentor Graphics, Cadence, and other vendors to help you synthesize and verify a design.
- CAES Logic Rules Checker and Tester Rules Checker allow you to verify partial or complete designs for compliance with CAES design rules.
- CAES HDL Design System accepts back-annotation of timing information through SDF.

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

XDT℠ (eXternal Design Translation)

Through CAES XDT services, customers can convert an existing non-CAES design to CAES processes. The XDT tool is particularly useful for converting an FPGA to an CAES radiation-tolerant gate array. The XDT translation tools convert industry standard netlist formats and vendor libraries to CAES formats and libraries. Industry standard netlist formats supported by CAES include:

- VHDL
- Verilog HDL™
- FPGA source files (Actel, Altera, Xilinx)
- EDIF
- Third-party netlists supported by Synopsys

Tools Supported by CAES

CAES supports libraries for:

- Mentor Graphics
  - QuestaSim
  - Tessent FastScan
  - Tessent MBIST
- Synopsys
  - Design Compiler (with Power Compiler)/Ultra
  - PrimeTime
  - PrimePower
  - Formality
  - TetraMax
- VITAL-compliant VHDL Simulation Tools
- OVI-compliant Verilog Tools

Training and Support

CAES personnel conduct training classes tailored to meet individual needs. These classes can address a wide mix of engineering backgrounds and specific customer concerns. Applications assistance is also available through all phases of ASIC Design.

Physical Design

Using five layers of metal interconnect, CAES achieves optimized layouts that maximize speed of critical nets, overall chip performance, and design density up to 3,000,000 NAND2 equivalent gates.

Test Capability

CAES supports all phases of test development from test stimulus generation through high-speed production test. This support includes ATPG, fault simulation, and fault grading. Serial scan design options are available on all UT0.25µHBD storage elements. Automatic test program development capabilities handle large vector sets for use with CAES LTX/Trillium MicroMaster, supporting high-speed testing (up to 80MHz with pin multiplexing), or Teradyne Tiger (up to 1.2GHz).

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Unparalleled Quality and Reliability

CAES is dedicated to meeting the stringent performance requirements of aerospace and defense systems suppliers. CAES maintains the highest level of quality and reliability through our Quality Management Program under MIL-PRF-38535 and ISO-9001. In 1988, we were the first gate array manufacturer to achieve QPL certification and qualification of our technology families. Our product assurance program has kept pace with the demands of certification and qualification.

Our quality management plan includes the following activities and initiatives.

- Quality improvement plan
- Failure analysis program
- SPC plan
- Corrective action plan
- Change control program
- Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV) assessment program
- Certification and qualification program

Because of numerous product variations permitted with customer specific designs, much of the reliability testing is performed using a Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV). CAES utilizes the wafer foundry's data from TCV test structures to evaluate hot carrier aging, electromigration, and time dependent test samples for reliability testing.

Data from the wafer-level testing can provide rapid feedback to the fabrication process, as well as establish the reliability performance of the product before it is packaged and shipped.

Radiation Tolerance

CAES incorporates radiation-tolerance techniques in process design, design rules, array design, power distribution, and library element design. All key radiation-tolerance process parameters are controlled and monitored using statistical methods and in-line testing.

Parameter	Radiation Hardness Assurance	Notes
Total Ionizing Dose (TID)	$1.0E5$ rad(SiO_2) $1.0E6$ rad(SiO_2)	1,2 1,3
Dose Rate Upset (DRU)	$>6.6E9$ rad(Si)/sec	4
Dose Rate Survivability (DRS)	No latchup observed to maximum dose rate of equipment configuration $>4.8E11$ rad(Si)/sec	5,8
Single Event Up-set (SEU)	$<1.2E-12$ errors per cell-day	6,7
Single Event Latchup (SEL)	Latchup-immune over worst case 125°C, 2.75V or 3.6V core, 3.6V I/O V_{DD}, LET $>108 MeV/cm^2/mg$	
Projected neutron fluence	$1.0E14$ n/sq cm	9

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Notes:

1) Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019.
2) Data sheet electrical characteristics guaranteed to 3.0E5 rads(SiO_2) with on-chip RAM. All post-radiation values measured at 25°C.
3) Datasheet electrical characteristics guaranteed to 1.0E6 rad (SiO_2) with on-chip RAM. All post-radiation values measured at 25°C.
4) Short pulse 20ns FWHM (full width, half maximum) 25°C, 2.25V core/3.0V I/O V_{DD}.
5) Short pulse 35ns FWHM (full width, half maximum) 125°C, 2.75V core/3.6V I/O V_{DD}.
6) SEU limit based on standard evaluation circuit at 2.25V or 3.6V core/3.0V I/O V_{DD} 25°C condition.
7) SEU-hard flip-flop cell. Non-hard flip-flop typical is 8E-9.
8) Dose rate upset number may be different for a specific design due to the size of the ASIC die.
9) Based on George C. Messenger, "A Summary Review of Displacement Damage from High Energy Radiation in Silicon Semiconductors and Semiconductor Devices," IEEE Trans Nucl. Sci, vol. 39, no. 3, June 1992.

Absolute Maximum Ratings [1]

(Referenced to V_{SS})

Symbol	Parameter	Limits
V_{DD} [2]	I/O DC Supply Voltage	-0.3V to 4.0V
V_{DDCORE} [2]	Core DC Supply Voltage	-0.3 to 2.8V or -0.3 to 4.0V
V_{DD} - V_{DDCORE}	Max Voltage Difference (2.5V core)	3.6V
V_{DDCORE} - V_{DD}	Max Voltage Difference (2.5V core)	2.8V
T_{STG}	Storage temperature	-65°C to +150°C
T_J	Maximum junction temperature	+150°C
I_{LU}	Latchup immunity	+150mA
I_I	DC input current	+10mA
T_{LS}	Lead temperature (solder 5 sec)	+300°C

Note:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) The recommended "power-on" sequence is V_{DDCORE} voltage supply applied first, followed by the V_{DD} voltage supply. The recommended "power-off" sequence is the reverse. Remove V_{DD} voltage supply, followed by removing V_{DDCORE} voltage supply.

Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD} I/O	DC Supply Voltage	3.3 ± 0.3V
V_{DDCORE} Core	DC Supply Voltage	2.5 ± 0.25V or 3.3 ± 0.3V

Note:

1) Under normal conditions, V_{DD} must be maintained at a voltage greater than V_{DDCORE} by 0.25V for 2.5V core option.

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

DC Electrical Characteristics

(V_{DD} = 3.3V ±0.3; V_{DDCORE} = 2.5V ±0.25 or 3.3V ±0.3V; -55°C<T_C<±125°C)

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage [1] CMOS, OSC inputs PCI inputs	V_{DD} = 3.3V ± 0.3V V_{DDCORE} = 2.5V ± 0.25V		0.3*V_{DD} 0.3*V_{DD}	V
V_{IH}	High-level input voltage [1] CMOS inputs PCI inputs	V_{DD} = 3.3V ± 0.3 V_{DDCORE} = 2.5V ± 0.25	0.7*V_{DD} 0.5*V_{DD}		V
V_{IL}	Low-level input voltage SSTL inputs	V_{DDSTL} = 1.8V + 10% V_{REF} = 0.9V	VREF - 0.125		V
V_{IH}	High-level input voltage SSTL inputs	V_{DDSTL} = 1.8V + 10% V_{REF} = 0.9v		VREF + 0.125	V
V_T^+	Schmitt Trigger, positive going threshold [1]	V_{DD} = 3.3V ± 0.3 V_{DDCORE} = 2.5V ± 0.25		0.7*V_{DD}	V
V_T^-	Schmitt Trigger, negative going threshold [1]	V_{DD} = 3.3V ± 0.3 V_{DDCORE} = 2.5V ± 0.25	0.3V_{DD}		V
V_H	Schmitt Trigger, typical range of hysterisis [2]		0.4		V
I_{IN}	Input leakage current CMOS and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors Inputs with pull-up resistors Cold Spare Inputs - Off Cold Spare Inputs - On	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS} V_{IN} = V_{SS} V_{IN} = V_{DD} V_{IN} = 0 to 3.6V V_{IN} = V_{DD} or V_{SS}	-1 10 -5 -120 -5 -5 -5	1 120 5 -10 5 5 5	µA
V_{OL}	Low-level output voltage [3] CMOS/LVTTL 4.0mA buffer CMOS/LVTTL 8.0mA buffer CMOS/LVTTL 12.0mA buffer CMOS/LVTTL 24.0mA buffer CMOS outputs (optional) CMOS outputs (optional) PCI outputs	I_{OL} = 4.0mA I_{OL} = 8.0mA I_{OL} = 12.0mA I_{OL} = 24.0mA I_{OL} = 1.0µA I_{OL} = 100.0µA I_{OL} = 1500.0µA		0.4 0.4 0.4 0.4 0.05 0.25 0.1 * V_{DD}	V

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Symbol	Parameter	Condition	MIN	MAX	Unit

V_{OH}	High-level output voltage[3]
	  CMOS/LVTTL 4.0mA buffer
	  CMOS/LVTTL 8.0mA buffer
	  CMOS/LVTTL 12.0mA buffer
	  CMOS/LVTTL 24.0mA buffer
	  CMOS outputs (optional)
	  CMOS outputs (optional)
	  PCI outputs
		I_{OH} = -4.0mA
		I_{OH} = -8.0mA
		I_{OH} = -12.0mA
		I_{OH} = -24.0mA
		I_{OH} = -1.0µA
		I_{OH} = -100.0µA
		I_{OH} = -500.0µA
			2.4
			2.4
			2.4
			2.4
			V_{DD} - 0.05
			V_{DD} - 0.35
			0.9 * V_{DD}
					V

V_{OL}	Low-level output voltage SSTL outputs	V_{DDSTL} = 1.8V - 10% I_{OL} = 12mA		0.7	V
V_{OH}	High-level output voltage SSTL outputs	V_{DDSTL} = 1.8V - 10% I_{OL} = -12mA	V_{DDSTL} - 0.5		V
I_{OZ}	Three-state output leakage current CMOS Cold Spare Inputs - Off Cold Spare Inputs - On	V_O = V_{DD} and V_{SS} V_{IN} = 0V and 3.6V V_{DD} = V_{SS} = 0 V_{DD} = V_{DD} = V_{SS}	-5 -10 -10	5 +10 +10	µA
I_{OS}	Output short-circuit current [2, 4]	V/OUT= I/O drive = 4mA I/O drive = 8Ma I/O drive = 12mA I/O drive = PCI V/OUT= I/O drive = 4mA I/O drive = 8mA I/O drive = 12mA I/O drive = PCI	3.0V@125°C 68mA 95mA 174mA 410mA 3.6V@-55°C -84mA -102mA -153mA -348mA	3.6V@-55°C 143mA 204mA 340mA 764mA 3.0V@125°C -30mA -47mA -92mA -230mA	mA

C_{IN}	Input capacitance [5]
	  LVDS inputs
	  SSTL inputs
		f = 1MHz @ 0V	4	15
				16
				15
					pF

C_{OUT}	Output capacitance [5] 4.0mA buffer 8.0mA buffer 12.0mA buffer 24.0mA buffer LVDS outputs SSTL outputs	f = 1MHz @ 0V		15 18 20 25 19 15	pF
C_{IO}	Bidirect I/O capacitance [5] 4.0mA buffer 8.0mA buffer 12.0mA buffer PCI bidirects	f = 1MHz @ 0V		15 18 25 13	pF

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{OD1}	Differential output voltage LVDS	RL = 100Ω	250	800	mV
V_{OS}	Offset voltage LVDS	RL = 100Ω	1.12	1.6	V
ΔV_{OD1}	Change in magnitude of V_{OD1} for complementary output states LVDS	RL = 100Ω		35	mV
ΔV_{OS1}	Change in magnitude of V_{OS1} for complementary output states LVDS	RL = 100Ω		25	mV
IOS LVDS	Output short circuit current LVDS	$V_{IN} = V_{DD}$, V_{OUT+} = 0V or V_{IN}=GND, $V_{OUT\ -}$ = 0.V		9.0	mA
I_{DDQ}	Quiescent Supply Current [6] Group A, subgroups 1,3	V_{DD} = 3.6V 200K gates 400K gates 600K gates 800K gates 1000K gates 1500K gates 2000K gates 2500K gates 3000K gates			50 100 150 200 250 375 500 625 750
	Group A, subgroup 2	V_{DD} = 3.6V 200K gates 400K gates 600K gates 800K gates 1000K gates 1500K gates 2000K gates 2500K gates 3000K gates			1 2 3 4 5 7.5 10 12.5 15
	Group A, subgroup 1 RHA Designator: M, D, P, L, R	V_{DD} = 3.6V 200K gates 400K gates 600K gates 800K gates 1000K gates 1500K gates 2000K gates 2500K gates 3000K gates			4 6 8 10 12 18 24 30 36

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).

2) Supplied as a design limit but not guaranteed or tested.

3) Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF*MHz.

4) CAES IOS specification - maximum of 1 second for any output to be shorted to ground or the maximum output voltage supply - exceeding this specification will reduce the DC current lifetime because of potential joule heating.

5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz @0V and a signal amplitude of ≤50mV RMS in a 144 CPGA package.

6) All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

Intel is a registered trademark of Intel Corporation
Mentor, Mentor Graphics, AutoLogic II, QuickSim II, QuickFault II, QuickHDL, QuickGrade II, FastScan, FlexTest, QuestaSim and DFT Advisor are registered trademarks of Mentor Graphics Corporation
Verilog and Leapfrog are registered trademarks of Cadence Design Systems, Inc.
Synopsys, Design Compiler, Test Compiler Plus, VHDL Compiler, Verilog HDL Compiler, TestSim and VSS are trademarks of Synopsys, Inc.

Data Sheet Revision History

Revision Date	Description of Change	Page(s)
8-22-16	Added CAES data sheet template. Removed Sun Design Support. Removed the VCS design support. Removed Mentor ModelSim tools and replaced with QuestaSim.	All 1 2 7
2-18	Updated export	14

Hardened-by-Design Standard Cell ASIC

UT0.25µHBD

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.