

Interfacing 3.3V PROM with 2.5V Memory Controller using a 16bit Logic Transceiver

1.0 Introduction

As integrated circuit (IC) semiconductor process feature sizes decrease, so do their operating voltage levels. Faster signal transitions and lower power dissipation are a direct result of the smaller technologies. The aerospace industry is moving towards the lower voltage processors to take advantage of the faster speed and lower power requirements. While faster speeds with less power dissipation is advantageous, not all components in the system, such as PROMs, have migrated to the lower operating voltages. This results in I/O voltage level incompatibility amongst components. This design note illustrates how to interface with nonvolatile memories (specifically the 256K 3.3V PROM) with a 2.5V memory controller using level shifting bus transceivers and dual LDO voltage regulator.

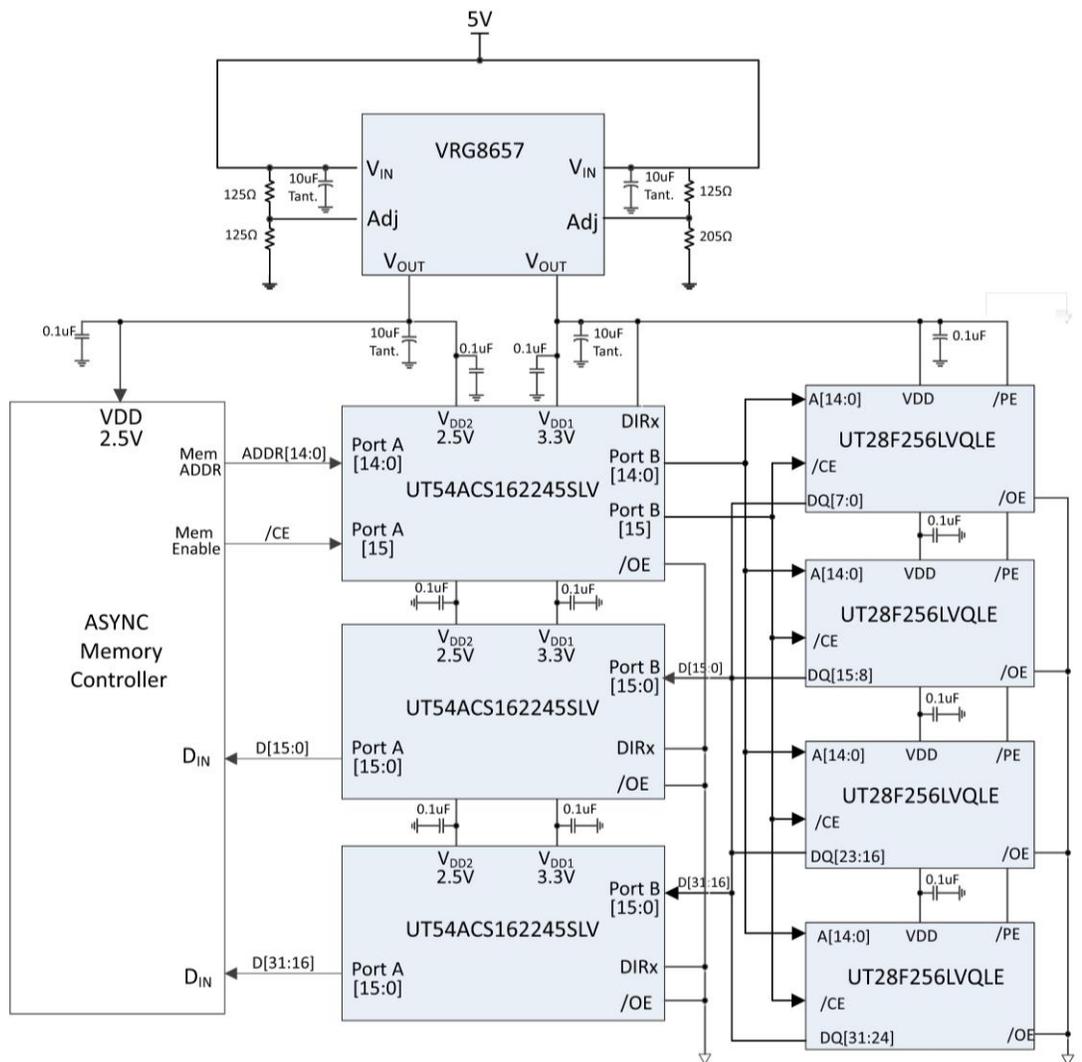


Figure 1. Block diagram 2.5V Asynchronous Memory Controller Interface with 3.3V PROM

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2.0 Design Implementation

Figure 1 depicts a block diagram interfacing with the UT28F256LVQLE 3.3V PROM with a 2.5V asynchronous memory controller port using the voltage translation feature of UT54ACS162245SLV 16-bit Bidirectional Multipurpose Low Voltage Transceiver. Assuming a 5V power source is present, the components supply voltages are regulated to meet both the 2.5V and 3.3V requirements using VRG8657 Dual Voltage Regulator. While this design note is specific for 3.3V PROM, the same concept applies for all 3.3V asynchronous memories such as SRAM, MRAM, and NOR Flash.

The controller sends address and control signal information to the PROM via the transceiver which translates the voltage from 2.5V up to 3.3V for PROM input. The PROM returns data to the controller through two additional transceivers which translate the 3.3V PROM data down to the controller's 2.5V I/O level.

The VRG8657 regulator is capable of providing 1 amp of current for each voltage level. The typical current requirements for both the 2.5V and 3.3V regulator operating at a 12.5MHz read cycle is estimated in the following calculations. Subsequent calculations assume the number of switching I/Os will be one half of the total number of I/Os.

2.1 Calculations for 2.5V Regulation Current

Total maximum power is specified for the transceiver at 3mW/MHz per switching output at 2.5V into a 40pF load. Since two of the transceivers will drive data from the 2.5V port into the controller, the maximum power is calculated as:

$$\begin{aligned} & (\text{Frequency in MHz}) (\# \text{ of switching I/Os}): \\ & (3\text{mW}) (12.5) (16) = 600\text{mW}; \\ I = P/V: 600\text{mW} / 2.5\text{V} & = 240\text{mA}. \end{aligned}$$

The switching power of the memory controller driving address and enable signals into the transceiver is calculated as:

$$\begin{aligned} P_{AVE} &= (C_{LOAD}) (V_{DD2}) (\text{Frequency}) (\# \text{ switching I/Os}) \\ P_{AVE} &= (15\text{pF}) (2.52) (12.5\text{MHz}) (8) \\ P_{AVE} &= 9.4\text{mW}; 9.4\text{mW} / 2.5\text{V} = 3.76\text{mA} \end{aligned}$$

Total 2.5V current is 244mA not including the current requirements of the memory controller.

2.2 Calculations for 3.3V Regulation Current

Total maximum power is specified for the transceiver at 6.2mW/MHz per switching output at 3.3V into a 40pF load (typical input capacitance of PROM address input is 10pF). One transceiver drives data from the 3.3V port into the PROMs.

$$\begin{aligned} & (6.2\text{mW}) (12.5) (8) = 620\text{mW}; \\ 620\text{mW} / 3.3\text{V} & = 188\text{mA} \end{aligned}$$

Typical power consumption for PROM is 30mW at 80ns read cycle time at 3.3V with $I_{OUT} = 0$. For four PROMs that equates to 120mW. Average switching power for the four PROMs driving 32 data bits is calculated as:

$$\begin{aligned} P_{AVE} &= (C_{LOAD}) (V_{DD2}) (\text{Frequency}) (\# \text{ switching I/Os}) \\ P_{AVE} &= (15\text{pF}) (3.32) (12.5\text{MHz}) (16) \\ P_{AVE} &= 32.6\text{mW} \end{aligned}$$

Total PROM current is $(120\text{mW} + 33\text{mW}) / 3.3\text{V} = 47\text{mA}$ ∴ Total 3.3V current is 235mA

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3.0 Conclusion

As IC process technologies advance, operating voltages are decreasing. While this increases signal process speeds and reduces power dissipation, it creates I/O level interface mismatches with other required components. This design note illustrates how to accomplish the voltage translation between a 2.5V memory controller and 3.3V 256K PROMs. Figure 1 illustrates this solution by using a VRG8657 dual voltage regulator, three UT54ACS162245SLV 16-bit bidirectional transceivers, and four UT28F256LVQLE PROMs for a x32 bit data bus configuration to maintain a high level of data integrity in radiation environments.

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