

Radiation Hardened and High Reliability Solutions



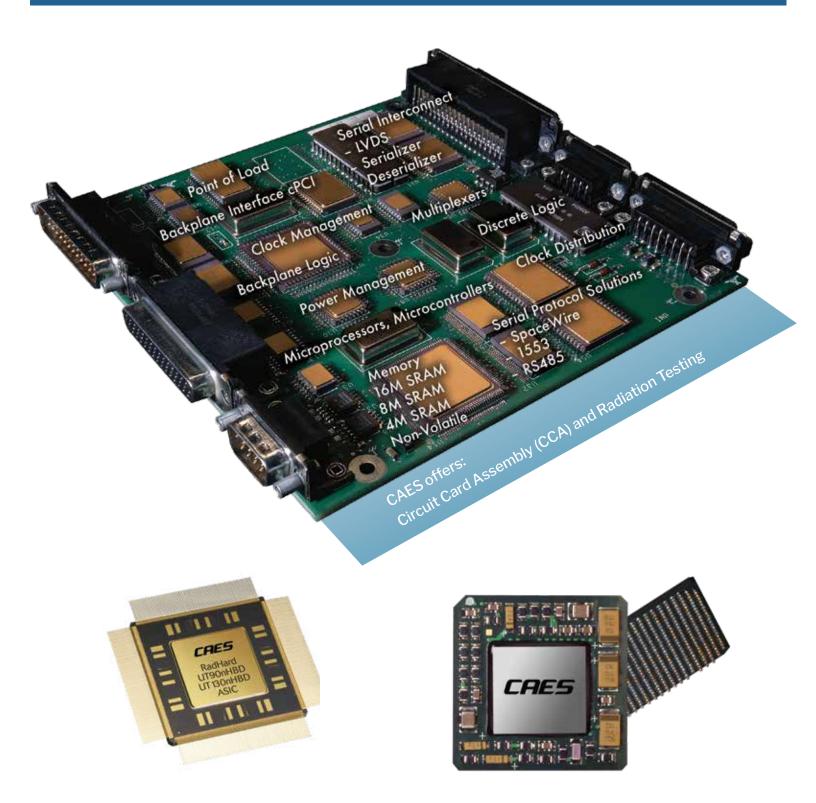






Product Short Form

CAES – offers digital, analog, and power Solutions for HiRel Applications with their standard and custom ASIC integrated circuits, IP, Circuit Card Assembly, Advanced Packaging and Radiation Effects Testing.



STANDARD PRODUCTS for HiRel APPLICATIONS

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LEON Microprocessors caes.com/HiRel	Description	70/6/10-	15/2-1-07/2-16/ 15/2-1-07/2-16/	Pochese	OMO	7\$} %0WS
GR740 Quad-Core LEON 4FT SPARC™ V8 32-bit	GR740 quad-core LEON 4FT 32-bit processor, with four fully SPARC V8 compliant integer units and four high performance fully pipelined IEEE-754 floating point units capable of running at up to 250 MHz. Connected through a 128-bit wide AMBA AHB bus to 2 MiB L2-cache, the four cores provide unparalleled throughput, performance and processing resources. The main memory interface is 64-bit PC100 SDRAM with Reed-Solomon EDAC protection, with a separate interface to boot-PROM memory	300†	60†	625 LGA, CGA	Q, V	5962-21204
Microprocessor with four IEEE- 754 floating point units	and I/O. The system is built around a total of five interconnected AMBA AHB buses. Communication interfaces include a SpaceWire router with eight 200 Mbit/s SpaceWire links, two 10/100/1000 Mbit Ethernet, 32-bit 33MHz PCI, MIL-STD-1553, two CAN ports, two UART, SPI and GPIO. Some interfaces share pins through internal multiplexers. The GR740 is part of the ESA roadmap for standard microprocessor components. Industry standard development tools are supported.	333	551	PGA‡	N/A	N/A
GR712RC Dual-Core LEON 3FT SPARC™ V8 32-bit Microprocessor	GR712RC is a dual-core LEON3FT 32-bit processor, with two fully SPARC V8 compliant integer units and two high performance fully pipelined IEEE-754 floating point units capable of running at up to 100 MHz, equating to 200 DMIPS and 200 MFLOPS throughput. GR712RC includes a memory controller with BCH and Reed-Solomon EDAC, 192 kByte on-chip memory with EDAC, 6 SpaceWire ports (2 with RMAP), 10/100 Ethernet, redundant Mil-Std-1553B BC/RT/BM interfaces, redundant CAN ports, CCSDS/ECSS TM/TC, SPI, I2C, 6 UARTs, JTAG debug port, etc. Some interfaces share pins through internal multiplexers. Industry standard development tools are supported.	100	≤118*	240 FP	**	***
UT700 32-bit Fault-Tolerant SPARC™ V8/LEON 3FT Processor	LEON 3FT 32-bit SPARC™ Microprocessor, fully SPARC™ V8 compliant integer unit, with 16kB of both instruction and data cache, capable of running up to a system clock speed of 166MHz, with 1.2 DMIPS / MHz performance. Includes a high performance fully pipelined IEEE-754 Floating Point Unit and Multi-functional Memory Controller. Integrated peripherals include MIL-STD-1553, SPI, 4 SpaceWire ports, 32bit/33MHz PCI, 10/100 Ethernet, 2 CAN ports, and 1 debug port. Industry standard development tools are supported.	100	≤110*	484 LGA, CGA	Q., V	5962-13238
UT699E 32-bit Fault-Tolerant SPARC™ V8/LEON 3FT Processor	LEON 3FT 32-bit SPARC™ Microprocessor, fully SPARC™ V8 compliant integer unit, with 16kB of both instruction and data cache, capable of running up to a system clock speed of 100MHz, with 1.2 DMIPS / MHz performance. Includes a high performance fully pipelined IEEE-754 Floating Point Unit and Multi-functional Memory Controller. Integrated peripherals include 4 SpaceWire ports, 32bit/33MHz PCI, 10/100 Ethernet, 2 CAN ports, and 1 debug port. Industry standard development tools are supported.	100	≤110*	484 LGA, CGA	Q, ,V	5962-13237
UT699 32-bit Fault-Tolerant SPARC™ V8/LEON 3FT Processor	LEON 3FT 32-bit SPARC™ Microprocessor, fully SPARC™ V8 compliant integer unit, capable of running up to a system clock speed of 66MHz, equating to a 89 DMIPs throughput. Includes a high performance fully pipelined IEEE-754 Floating Point Unit and Multi-functional Memory Controller. Integrated peripherals include 4 SpaceWire ports, 32bit/33MHz PCI, 10/100 Ethernet, 2 CAN ports, and 1 debug port. Industry standard development tools are supported. Flight heritage.	100	≤108*	352 FP and 484 LGA, CGA	Q, ,V	5962-08228

- * Contact factory for SEU report
- ** Class S screening and qualification
- *** Per CAES procurement specification
- ‡The plastic GR740 (PBGA) has all the same features as the ceramic package option, with the exception of the temperature range, which is -40°C to 105°C and qualification in accordance with ESCC-Q-60-13C Class 2. Prototypes (GR740-CP-PBGA625) and flight models (GR740-AS-PBGA625) are available now.
- † SEL immunity up to LET = 60 MeV cm2/mg at 125°C Tj and maximum VDD provided by technology. TID up to 300 krad(Si) provided by technology. See https://gaisler.com/GR740 for latest radiation test results.





LEON Microprocessor Eval **Boards**

caes.com/HiRel

Description

GR-CPCI-GR740 Development Board

The GR-CPCI-GR740 development board has been designed to support the development and fast prototyping of systems based on the CAES Gaisler GR740 quad-core 32-bit fault tolerant LEON4FT SPARC V8 processor. The board supports MIL-STD-1553B, 10/100/1000 Base-T Ethernet, eight SpaceWire ports, 32-bit PCI, two CAN ports, two UARTs, Serial Peripheral Interface, on-board Flash and SDRAM. On-board USB and SpaceWire debug ports are also available.

GR-VPX-GR740 Development board

The GR-VPX-GR740 development board has been designed to support the development and fast prototyping of systems based on our GR740 quad-core 32-bit fault-tolerant LEON4FT SPARC V8 processor supporting Open VPX and SpaceVPX environments. The GR-VPX-GR740 board comes in a 6U VPX format (233.5 mm x 160 mm) and is intended for use in OpenVPX chassis occupying a 1" slot (including mezzanine board). The board can also be used in stand-alone operation with a single 12V supply, in this case with limited VPX functionality. The board is equipped with on-board memories for boot and application storage, and an SODIMM for SDRAM. The front panel includes basic communication interface and LED indicators, whereas the rear connectors are intended for OpenVPX/SpaceVPX backplane connections.

GR712RC-BOARD Dual-Core LEON 3FT Development Board

The GR712RC-BOARD evaluation board is capable of running at a system clock speed of 100MHz. The board is a double Eurocard form factor used in a standalone bench-top configuration. The board supports MIL-STD-1553B, 10/100 Base-T Ethernet, six SpaceWire ports capable of running at up to 200Mbits/s, two CAN ports, on-board FLASH, SRAM, and SDRAM. A USB debug port is also available on-

GR-CPCI-UT699 Fault-Tolerant SPARC™ V8 Processor ASIC **Evaluation Board**

Development board with the UT699 LEON3FT SPARC V8 microprocessor. The board is cPCI form factor and can also be used in a standalone bench-top configuration. The board supports 32-bit/33MHz PCI, Ethernet, 4 SpaceWire ports capable of running up to 200Mbit/s, 2 CAN ports, on-board FLASH, SRAM, SDRAM, and socket for a PROM device. A USB debug port is provided.

4250252-00x UT700 LEAP with or without MEZ 43502740-000 - MEZ (Mezzanine Card) Only

The CAES LEAP provides a flexible development platform for customers wanting to develop software that works on the CAES UT700 Standard Product with minimal cost investment. The CAES LEAP has a CAES UT700 LEON 3 FT prototype grade device with 8 Mbytes $NV\ memory\ storage\ and\ 32Mbytes\ SDRAM\ (both\ commercial\ memory),\ along\ with\ one\ USB\ UART\ interface\ and\ one\ 10T/100\ Mbit/s$ Ethernet port. It also includes a JTAG interface for programming and debug of UT700 LEON 3FT (requires XILINX USB Platform Cable) along with one 192-pin mezzanine card expansion connector and an on-board Programmable LEAP main clock. The optional Mezzanine (Mez) card has an SPI display, two CAN bus, two SpaceWire and a dual-redundant CHA/CHB 1553B.



Gen 6 LEON 3FT Single Board Computer (SBC) caes.com/HiRel

GEN 6 LEON 3FT 3U cPCI SBC is a flight ready TRL-8 board for LEO, GEO and Planetary Missions. Flexible Architecture, enabled for use of LEON 3FTs Microprocessors, including the UT699, UT699E, UT700. It supports up to 95 Dhrystone MIPS performance with a 132MHz System Clock. On board memory supported is 64MB of SRAM Memory and 32MB of NV Memory, along with two cPCI bus I/F connectors (Hypertronics) and two SpW connectors. IPC-6012 Class 3A compliance.

With our Electronic Manufacturing Service (EMS) experience on the LEAP board, and various flight board builds, CAES can serve your needs with an off-the-shelf Single Board Computer (SBC) option specifically designed for Command and Control Applications.

DS4350272-x00	UT699E	33	33	33 / 0 W-S	44.2	33	3.0	5.1
DS4350272-x01	UT699E	66	66	66/3W-S	70.4	132	3.5	6.6
DS4350272-x02	UT700	33	33	33/0 W-S	44.2	33	3.0	5.1
DS4350272-x03	UT700	66	66	66/3W-S	70.4	132	3.5	6.6
DS4350272-x04	UT700	132	66	66/3W-S	94.9	132	4.2	7.3

Conditions: cPCI active/Memory Access [Typ = no Access | Max = 50% All other IP Functions Disabled via Clock gating register.

GEN VI Single Board Computer EM, FM Designations

Several models of the GEN VI SBCs can be manufactured based on usage purpose, delivery schedule, mass, and cost. The following types of assemblies are identified: a) Flight Modules (FM): Designated by a -3xx in the part number, the FMs are used in spacecraft final production. These units meet full specifications.

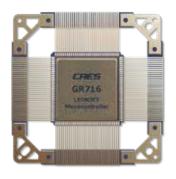
b) Engineering Model (EM): Designated by a -1xx in the part number, the EMs are flight-like units used in the flight design checkout, software development and qualification, upper assembly unit checkout and initial flight unit integration (pre-environmental). EMs meet full design specifications less the Flight Parts and board level environmental tests/ screening. Contact factory for other flows besides EM and FM, i.e. "Flight Lite".

Rad Tolerant Arm® Cortex® Microcontroller and Eval Board caes.com/HiRel	0,00	May 6	2000 MH2)	Poliphora's	Memory	800 B		(S/be, 137)	MO COLLINS	ons on
UT32M0R500 (Ceramic)	MO+	50	DAC ADC Comparator	CAN I2C SPI PWM UART GPIO	NOR Flash SRAM	143 pin CLGA, CBGA, CCGA 14.5 x 14.5 mm, 1 mm pitch	50	80	Q,Q+	5962-17212
UT32M0R500 (Plastic)	MO+	50	DAC ADC Comparator	CAN I2C SPI PWM UART GPIO	NOR Flash SRAM	143 pin PBGA 14.5 x 14.5mm, 1 mm pitch	50	80	NA	NA
UT32M0R500-EVB	Uno co board i	nnectivi	ty and full product	pinout allow fo	r easy expansion	orm for the UT32M and accessibility. T connectors for co	Along	with the r	microcontro	ller, the subject

Contact factory for recommendations on software environment (IDE) and API drivers.







LEON Microcontroller and Eval Board caes.com/HiRel	Description		(Shen 200 17-17-16)	Pack	%8 O'alli _{G3*} ;	5MD*
GR716A	The GR716A features a 50MHz fault-tolerant, single-core LEON3FT SPARC V8, 32-bit instruction set processor with support for LEON-REX 16-bit compressed mode, with various communication interfaces (Spacewire, CAN 2.0B, MIL-STD-1553, SPI, I2C) and on-chip ADC (2xADC, 11-bit resolution), DAC (12-bit resolution at 3 Mbps, 4 channels), programmable PWM, on-chip temperature sensor, Power-on-Reset, oscillator, brownout detection, LVDS transceivers, and on-chip LDO and integrated PLL. This microcontroller is ideally suited for space and other high-rel applications, such as satellite supervision, monitoring and distributed control.	100	≤118	132 QFP 24mm X 24mm	ESCC 9000	N/A
GR716B	The GR716B is an enhanced version of the GR716A microcontroller with the same features in he same package, but running at twice the speed (100MHz), with support for SRAM & SPI (on memory interface). Additional features include support for 4-byte address mode on the external SPI memory interface, hardware FPGA programming and scrubber, 2 port SpaceWire router, 2 x CAN-FD (CANopen support for remote boot), enhanced PWM interface, 10/100 Ethernet, programmable enhanced DMA, 4 x ADC (13-bit resolution), LVDS with cold spare & fail safe support, and 20x analog comparator.	100	≤118	132 QFP 24mm X 24mm	ESCC 9000	N/A
GR-CPCI-GR716-DEV	The GR716 Interface Development board is a motherboard, that requires the GR716 dat this daughter card). It is a 233mm X 160mm, 6U cPCl format board with 2 slot wide fron support for SpaceWire (LVDS), GPIO (64 pins), FTDI USB interface). Expansion is possib UARTs, CAN, 1553, SPI). Expansion slot for memory or user defined functions. Sockete and PWM clocks.	t panel (fr le throug	ont panel h various	interfaces in accessory bo	nclude pards (for	
GR716-BOARD	Development board for the GR716 LEON3 microcontroller. The board has a small form f debug link, an SPI Flash ROM (32MB) and a socket oscillator. Moreover, the PCI-104 hea user-defined modules (memory, digital I/O and analogue I/O) or to the GR-CPCI-GR716-	iders (2x 6	64 pins) p	rovide an inte		

Non-Volatile Memories caes.com/HiRel	Config	ojjejno) Volt.	4 _{CQ}	10, 10, 10, 10, 10, 10, 10, 10, 10, 10,	LETTHOSE WASH	Salurated Co. 20	Laten-Uni	CMOS MANNERS	shouts 17	shaw, Sed	986. WO	%0%/ %0%
UT8MR2M816M MRAM	2M x 8	3.3V	45 ns	1000	N/A*	N/A*	>100	X		40 FP	Q,V	5962-12227
UT8MR8M8 64M MRAM	8M x 8	3.3V	50 ns	1000	N/A*	N/A*	>100	X		64 FP	Q,V	5962-13207
UT8QNF8M8 64M NOR Flash	8M x 8 and 4M x 16	3.3V	60 ns	10 and 50**	29	5.0E-13	>80	Χ		48 FP	Q,Q+	5962-12204
UT28F64 PROM	8K x 8	5V	35 ns	1000	100	1.0E-11	>100		Χ	28 FP 28 DIP	Q,V	5962-96873
UT28F64LV PROM	8K x 8	3.3V	55 ns	1000	100	1.0E-11	>100		X	28 FP 28 DIP	Q,V	5962-01516
UT28F256LVQLE	32K x 8	3.3V	65 ns	100- 1000	50	2.5E-6***	>100		X	28 FP	QV	5962-01517
UT28F256QLE	32K x 8	5V	45 ns	100- 1000	50	9.4E-7***	>100		X	28 FP	QV	5962-96891

[†] Contact factory for availability. Not recommended for new designs.

* Upset immune at LET of 112 MeV-cm2/mg.

** Device 10% powered on and 90% powered off.

*** Saturated Cross Section (cm2) per device.

SONOS RadHard NOR Flash caes.com/HiRel	Merina	Config	10/19/80s	Acese	only Coleto	(Speyes Now	A See See See See See See See See See Se	mo mo	A. / Mg
UT81NFR8M8 64Mb NOR Flash	Parallel	8M x 8	1.8V-3.6V	60 ns	300	≤80	48 FP	Q, Q+, V	5962-21210
UT81NFR64M1 64M NOR Flash	SPI	64M x 1	1.8V-3.6V		300	≤80	20 FP	Q, Q+, V	5962-21209
UT81NFR128M8 1G NOR Flash	Parallel	128M x 8	1.8V-3.6V	60 ns	300	≤80	142 pin CCGA, CBGA, CLGA	Q, Q+, V	5962-21210
UT81NFR1G11G NOR Flash	SPI	1G x 1	1.8V-3.6V		300	≤80	142 pin CCGA, CBGA, CLGA	Q, Q+, V	5962-21209

[†] Contact factory for availability. Not recommended for new designs.

* Upset immune at LET of 112 MeV-cm2/mg.

** Device 10% powered on and 90% powered off.

*** Saturated Cross Section (cm2) per device.

FPGAs caes.com/FPGA	Description	Solo Solo Solo Solo Solo Solo Solo Solo
UT24C407	Certus [™] -NX-RT	39 2.5 100 80 Space Automotive
UT24C1007†	CertusPro TM -NX-RT	96 7.3 100 80 Space Automotive

[†] Contact factory for availability

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Volatile Memories	Configure	10 CO VIEW		**************************************	Ser JANON	Solution (1982)	CMC CMMMs	17.17.15.15.15.15.15.15.15.15.15.15.15.15.15.	100	300*
caes.com/HiRel	S	3/2	A.	\ \lambda^{\alpha}	7 %	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		2 20	\Q	25
Monolithics										
UT8R512K8 SRAM	512K x 8	3.3V, 1.8V	15 ns	300	50	1.7E-7	≤100	36 FP	Q, V	5962-03235
UT8ER512K32 SRAM	512K x 32	3.3V, 1.8V	20 ns	100	N/A**	N/A**	≤100	68 FP	Q, V	5962-06261
UT8R128K32 SRAM	128K x 32	3.3V, 1.8V	15 ns	300	50	1.7E-7	≤100	68 FP	Q, V	5962-03236
UT8Q512E 4M SRAM	512K x 8	3.3V	20 ns	50	50	2.8E-8	≤100	36 FP	Q, V	5962-99607
UT9Q512E 4M SRAM	512K x 8	5V	20 ns	50	50	2.8E-8	≤100	36 FP	Q, V	5952-00536
UT7C138/139RH Dual-Port SRAM	4K x 8/9	5V	45 ns	1000	85	3.8E-8	≤100 ■	68 FP and 68 DIP	Q, V	5962-96845
Multi-Chip Modules (MCMs)										
UT8SDMQ64M48 3.0Gb SDRAM	64M x 48	3.3V	7.5 ns	100	21	7.6E-10	≤100	128 FP	Q, Q+	5962-10230
UT8SDMQ64M40 2.5Gb SDRAM	64M x 40	3.3V	7.5 ns	100	21	7.6E-10	≤100	128 FP	Q,Q+	5962-10229
UT8ER4M32128M SRAM	4M x 32	2.5V or 3.3V, 1.8V	25 ns	100	N/A**	N/A**	≤100	132 FP	Q,Q+	5962-10204
UT8ER2M32 64M SRAM	2M x 32	2.5V or 3.3V, 1.8V	22 ns	100	N/A**	N/A**	≤100	132 FP	Q,V	5962-10203
UT8ER1M32 32M SRAM	1M x 32	2.5V or 3.3V, 1.8V	20 ns	100	N/A**	N/A**	≤100	132 FP	Q,V	5962-10202
UT8R4M39160M SRAM	4M x 39	2.5V or 3.3V, 1.8V	25 ns	100	15	8.0E-8	≤100	132 FP	Q,Q+	5962-10207
UT8R2M39 80M SRAM	2M x 39	2.5V or 3.3V, 1.8V	22 ns	100	15	8.0E-8	≤100	132 FP	Q,V	5962-10206
UT8R1M39 40M SRAM	1M x 39	2.5V or 3.3V, 1.8V	20 ns	100	15	8.0E-8	≤100	132 FP	Q,V	5962-10205
UT8CR512K32 SRAM	512K x 32	3.3V or 1.8V	17 ns	300	50	1.7E-7	≤100	68 FP	Q,V	5962-04227
UT8Q512K32E16M SRAM	512K x 32	3.3V	25 ns	50	50	2.8E-8	≤100	68 FP	Q,V	5962-01533
UT9Q512K32E16M SRAM	512K x 32	5V	25 ns	50	50	2.8E-8	≤100	68 FP	Q,V	5962-01511

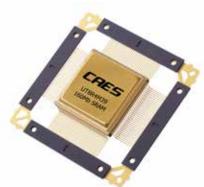
† Contact factory for availability. Not recommended for new designs.

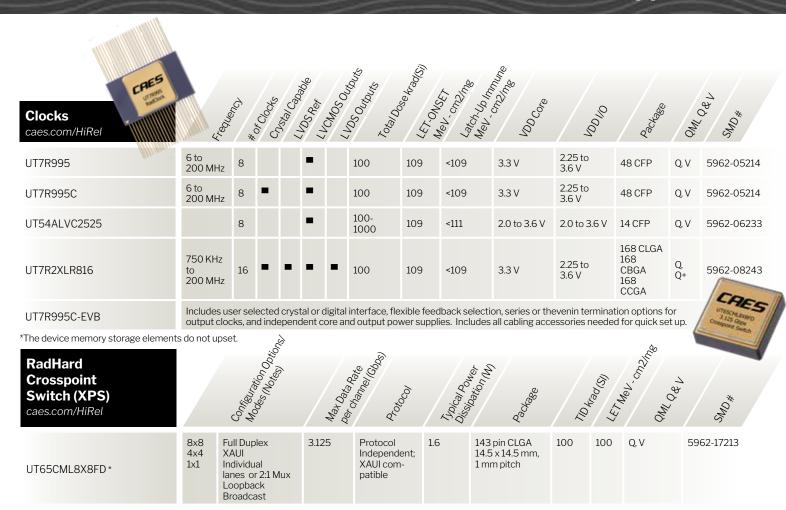
* The SEU error rate is driven by particle flux and internal error correction is 1x10-15 errors/bit-day.

** The SEU error rate is driven by particle flux and EDAC scrub rate. At the default scrub rate the error rate is 8.1x10-16 errors/bit-day.

*** Device QMLQ, Q+ qualified. SMD publication pending. Contact factory for status.







Notes:

- $1) 1 \\ Input Channel (e.g. Bank 0, Side A) to 1 \\ or 2 \\ Output Channels (e.g. Bank 2 \\ and/or Bank 3, Side B) \\ \\ refer to figures in the data sheet. \\$
- 2) 1-4 Input Channels (e.g. Bank 0, Side A) to 1-4 or 1-8 Output Channels (e.g. Bank 2 and/or Bank 3, Side B). Specific Input Channels to specific Output Channels only; does not support any Input Channel to any Output Channel
- 3) 2:1 MUX/Selector function
- 4) Supports CML + LVDS I/O Logic Standards (differential signals)

^{*} Contact factory regarding a Development board.

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RadHard SpaceWire caes.com/HiRel	Link	Doto Rates		1/6/0/	250 Had S.)	Saturated Cigs	(7), 00, 00, 00, 00, 00, 00, 00, 00, 00, 0		mo	7\$; 8M0,*
GR718B 18-port SpaceWire Router	18	200	3.3V, 1.8V	300	**	**	≤80	256 CQFP	***	†
GR718B Evaluation Board	ports 1	8 SpaceWire	ports capable o	of running u	aluation board and p to 200Mbit/s th ports are driven by	rough front-pane	el MDM9S conne	ectors. Two Spac	eWire por	ts are driven by
UT200SpWPHY01 SpaceWire Physical Layer Transceiver	1	200	3.3V	100	38	5.0E-7	≤109	28 FP	Q, V	5962-06232
UT200SpW4RTR SpaceWire 4-port Router	4	200	2.5V, 3.3V	100	26	*	≤100	255 CLGA	Q, V	5962-08244
UT200SpW4RTR-EVB 4-port Router Evaluation Board	tures o	fthe UT2009		ceWire 4-p	Vire Router evalua ort Router as defir					
UT100SpW02 SpaceWire Protocol Handler IP					gned specifically fo smit and receive F			se FPGA. Dual EC	SS-E-ST-5	50-KC compliant

^{*} Contact factory for SEU report

^{**} The SEU error rate is below 1E-12 errors/bit-day

^{***} ESCC 9000 screening and lot validation.

[†] Per CAES procurement specification.

			Tri mous	outs)	88	Spens	187°.
LVDS caes.com/HiRel	Description	/5	SOM	Sindy?	7/6/0/	000	* WS
UT54LVDS031 Quad Driver*	Operates at >155.5 Mbps (77.7 MHz) switching ranges with ultra low power CMOS technology.		X	16 FP	300-1000	Q, V	5962- 95833
UT54LVDS032 Quad Receiver*	Operates at >155.5 Mbps (77.7 MHz) switching ranges with ultra low power CMOS technology. Receiver fail-safe.		X	16 FP	300 -1000	Q, V	5962- 95834
UT54LVDSC031 Quad Driver*	Operates at >155.5 Mbps (77.7 MHz) switching ranges with ultra low power CMOS technology. Cold spare all LVDS outputs.		Х	16 FP	300	Q, V	5962- 95833
UT54LVDSC032 Quad Receiver*	Operates at >155.5 Mbps (77.7 MHz) switching ranges with ultra low power CMOS technology. Receiver fail-safe. Cold spare all LVDS inputs.		X	16 FP	300	Q, V	5962- 95834
UT54LVDS031LV/E Quad Driver	Operates at >400.0 Mbps (200 MHz) switching ranges with ultra low power CMOS technology. Cold spare all pins.	Χ		16 FP	300 -1000	Q, V	5962- 98651
UT54LVDS032LV/E Quad Receiver	Operates at >400.0 Mbps (200 MHz) switching ranges with ultra low power CMOS technology. Receiver fail-safe. Cold spare all pins.	X		16 FP	300 -1000	Q, V	5962- 98652
UT54LVDS217 Serializer	15 to 75 MHz shift clock support, power-down mode <60 μA (max), narrow bus reduces cable size and cost, cold spare all pins.	Χ		48 FP	300 -1000	Q, V	5962- 01534
UT54LVDS218 Deserializer	15 to 75 MHz shift clock support, power-down mode <60 μA (max), narrow bus reduces cable size and cost, cold spare all pins.	Χ		48 FP	300 -1000	Q, V	5962- 01535
UT54LVDS328 Octal Repeater	Operates at >400.0 Mbps (200 MHz) with 10mA LVDS output drivers. Cold spare all pins.	X		48 FP	300 -1000	Q, V	5962- 01536
UT54LVDM328 Octal Bus Repeater	Operates at >400.0 Mbps (200 MHz) with 10mA LVDS output drivers. Cold spare all pins.	Χ		48 FP	300 -1000	Q, V	5962- 01536
UT54LVDM228 Quad 2x2 Crosspoint Switch	Operates at >400.0 Mbps (200 MHz) with 10mA LVDS output drivers. Cold spare all pins. Configurable as quad 2:1 mux, 1:2 demux, repeater or 1:2 signal splitter.	X		64 FP	300 -1000	Q, V	5962- 01537
UT54LVDS032LVT Low Voltage Quad Receiver with Integrated Termination Resistor*	Operates at >400.0 Mbps (200 MHz) switching ranges with ultra low power CMOS technology, nominal 105 ohms integrated termination resistor. Cold spare all pins.	X		16 FP	300 -1000	Q, V	5962- 04201
UT54LVDM031LV Low Voltage Bus LVDS Quad Driver	Operates at >400.0 Mbps (200 MHz) with 10mA LVDS output drivers. Cold spare all pins.	X		16 FP	300	Q, V	5962- 06201
UT54LVDM055LV Dual Driver and Receiver	Operates at >400.0 Mbps (200 MHz) with 10mA LVDS output drivers. Receiver fail-safe. Cold spare all pins.	X		18 FP	300	Q, V	5962- 06202

^{*} Not recommended for new designs





			1111				
Controller Area Network (CAN) Flexible Data Rate (FD) Transceivers* caes.com/HiRel	Description	Bauchale	, otal Dose ,	Media (Control of the Control of the	%	mo	2M8*
UT64CAN3330	Controller Area Network (CAN) Transceiver - Sleep Mode	10 kbps to 8 Mbps	100	117	8 FP	Q, V	5962-15232
UT64CAN3331	Controller Area Network (CAN) Transceiver - Diagnostic Loopback Mode	10 kbps to 8 Mbps	100	117	8 FP	Q, V	5962-15232
UT64CAN3332	Controller Area Network (CAN) Transceiver - Auto-baud Loopback Mode	10 kbps to 8 Mbps	100	117	8 FP	Q, V	5962-15232

^{*} Evaluation board available. Contact factory.

MIL-STD-1553 Databus caes.com/HiRel	MI,570,153,8 MI,570,153,8 MI,670,173,153,8 MI,670,00,153,151,151,150,00,151,151,151,151,151,151,	5 2 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	Associate Remote Series Remote Series	Onitor 'ninal Dual Redundant 8-bit I/O	16-bit 10	Fatback	Ping	LCC Array	Application Option	S. Mo	780
UT69151 SµMMIT™ E		-		- -	1	132	84		HR1, AV	Q,V	5962-92118
UT69151 SµMMIT™ LXE*	- -	- -			1	100	96		HR2, AV	Q,V	5962-94663
UT69151 SµMMIT™ DXE	-			- -	1	100	96		HR1, AV	Q,V	5962-94663
UT69151 SµMMIT™ XTE	- -				n	140	139		AV	Q	5962-94758
UT69151 SµMMIT™ RTE			-		1	132,140	139		AV	Q	5962-98587
UT1553B BCRT*	- -	-		- -	1	84	84		AV	Q	5962-88628
UT1553B BCRTB**	- -	-	-			84	84		AV	Q,V	5962-88628
UT1553B BCRTM*	- -	-		- -	1	84	84		AV	Q	5962-89577
UT1553B BCRTMB**	- -	-				84	84		AV	Q,V	5962-89577
UT1553 BCRTMP**	- - -	-		- -	•	132	144		AV	Q	5962-89501
UT1553B RTI*	- -	-	-	- -	1	84			AV		M38510/55501
UT1553 RTMP*	- - -	-	-	- -	•	84	84	84	AV	Q	5962-88645
UT1553B RTR*	- -	-	-	- -	-		68		AV	Q	5962-89576

^{*} Obsolete: Obsolete products have run out of supply, CAES can no longer produce obsolete products.
** End of Life (EOL): EOL products have reached a limited supply status and are not recommended for new designs.

MIL-STD-1553/ RS485 Transceivers caes.com/HiRel	PS 485	475/4	1/5%	$\gamma_{\mathcal{E}_{\lambda}}$	Dust Red	tuojun.	(Sheen)	400//cation 001/00/00/	S. MO	5W0 *
UT63M147 Bus Transceiver	-		-		•	1000	24 FP 36 DIP	HR3	Q,V	5962-93226
UT63M1x5C Bus Transceiver*	■ 1553A	-	-		-		24 DIP 36 FP 36 DIP	AV		
UT63M143 Bus Transceiver	•			-	-	1000	24 FP 36 DIP	HR3	Q,V	5962-07242
DRS4485 RS485/422 Dual Transceiver	-		-		•	100	18 FP		K	5962R09226

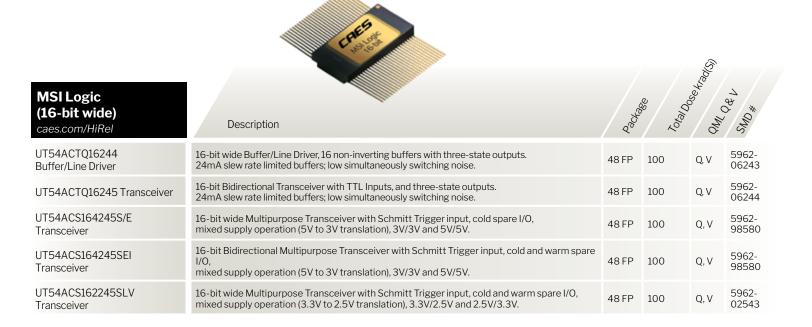
 $^{^{\}star}$ End of Life (EOL): EOL products have reached a limited supply status and are not recommended for new designs.

Application Options	Oranosoka	LETHORS	581, 188 581, 194 5851, 197 5851, 1975	MeV-CMM MeV-CM2M2 MeV-CM2M	
HR1	300*	42	1.5E-4	≤128	
HR2	100*	42	1.5E-4	≤128	
HR3	1000*	**	**	≤ 111	
HR4	N/A	N/A	N/A	N/A	· · · · · · · · · · · · · · · · · · ·

^{*} Maximum tolerance for product. Reduced tolerance products may be available. ** Device has no memory storage elements to upset.

RadTol Eclipse FPGAs caes.com/HiRel	SRAME	\$10 / 5/60/	10th/O	120 A 20 A	Solution Co. Solut	Car to Volume	M. W.	98. July 200	OMO	1 * 0ns
UT6325*	55K	1536	300	>42 logic cell flip flops >64 embedded SRAM	5.0E-7 2.0E-7	≤120	99 I/O, 25 input 163 I/O, 25 input 316 I/O, 25 input	208 CQFP 288 CQFP 484 CCGA	Q, V	5962- 04229
UT6325 Commercial*	55K	1536	300	>42 logic cell flip flops >64 embedded SRAM	5.0E-7 2.0E-7	≤120	99 I/O, 25 input 163 I/O, 25 input 310 I/O, 25 input	208 PQFP 280 PBGA 484 PBGA	Q, V	N/A
UT100SpW02 SpaceWire IP Protocol Handler				re Protocol Handler IP is rates from 2 to 100 Mbit					ECSS-E-	

^{*} End of Life (EOL): EOL products have reached a limited supply status and are not recommended for new designs.





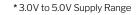
MSI ManyGate Devices caes.com/HiRel	Type Description	5.5.	10.5°	70/0/D	Npat B.	Syllic Online	OM OM	240 * OK
UT54ACS2S99S	Pin-configurable Logic Solution. Dual, Sequential, Configurable Logic Gate w/ Schmitt Trigger Inputs and Tri-state outputs. Also supports configuration as a D-flip flop (1R99S) or transparent latch (1L99S).	•	20 FP	1000	Schmitt CMOS	12mA	QV	5962-15239
UT54ACS3G99S	Pin-configurable Logic Solution. Triple, Combinatorial, Configurable Logic Gate w/ Schmitt Trigger Inputs and Tri-state outputs.		20 FP	1000	Schmitt CMOS	12mA	Q,V	5962-15238

MSI Logic

Standard Microcircuit Drawing (SMD) to CAES Colorado Springs Part Number caes.com/HiRel

•	Starraar a mile	John Gart Brawing	SIND, to of the Colorado
	SMD#	CAES Part #	Description
	5962-96512 5962-96512 5962-96513 5962-96513	UT54ACS00 * UT54ACS00E UT54ACTS00 * UT54ACTS00E	Quadruple 2-Input NAND Gates
	5962-96514 5962-96514 5962-96515 5962-96515	UT54ACS02 * UT54ACS02E UT54ACTS02 * UT54ACTS02E	Quadruple 2-Input NOR Gates
	5962-96516 5962-96516 5962-96517 5962-96517	UT54ACS04 * UT54ACS04E UT54ACTS04 * UT54ACTS04E	Hex Inverters
	5962-96518 5962-96518 5962-96519 5962-96519	UT54ACS08 *UT54ACS08E UT54ACTS08 *UT54ACTS08E	Quadruple 2-Input AND Gates
	5962-96524 5962-96524 5962-96525 5962-96525	UT54ACS14 *UT54ACS14E UT54ACTS14 *UT54ACTS14E	Hex Inverter Schmitt Trigger
	5962-96534 5962-96534 5962-96535 5962-90535	UT54ACS74 *UT54ACS74E UT54ACTS74 *UT54ACTS74E	Dual D Flip-Flops with Clear & Preset
	5962-96536 5962-96537	UT54ACS85 UT54ACTS85	4-Bit Comparators
	5962-96538 5962-96538 5962-96539	UT54ACS86 *UT54ACS86E UT54ACTS86	Quadruple 2-Input Exclusive OR Gates
	5962-96542 5962-96542 5962-96543 5962-96543	UT54ACS132 *UT54ACS132E UT54ACTS132 *UT54ACTS132E	Quadruple 2-Input NAND Schmitt Triggers
	5962-96544 5962-96544 5962-96545	UT54ACS138 *UT54ACS138E UT54ACTS138	3-Line to 8-Line Decoders/Demultiplexers
	5962-96552 5962-96553 5962-96553	UT54ACS157 UT54ACTS157 *UT54ACTS157E	Quadruple 2 to 1 Multiplexers

SMD#	CAES Part #	Description
5962-96554 5962-96555	UT54ACS163 UT54ACTS163	4-Bit Synchronous Counters
5962-96556 5962-96556 5962-96557 5962-96557	UT54ACS164 * UT54ACS164E UT54ACTS164 * UT54ACTS164E	8-Bit Shift Registers
5962-96564 5962-96564 5962-96565	UT54ACS191 *UT54ACS191E UT54ACTS191	Synchronous 4-Bit Up-Down Binary Counters
5962-96566 5962-96566 5962-96567 5962-96567	UT54ACS193 *UT54ACS193E UT54ACTS193 *UT54ACTS193E	Synchronous 4-Bit Up-Down Dual Clock
5962-96753	UT54ACTS220	Clock & Wait-State Generation Circuit
5962-96568 5962-96569	UT54ACS240 UT54ACTS240	Octal Buffers w/Inverted Three-State Outputs
5962-96570 5962-96570 5962-96571 5962-96571	UT54ACS244 *UT54ACS244E UT54ACTS244 *UT54ACTS244E	Octal Buffers & Line Drivers, Three-State Outputs
5962-96572 5962-96572	UT54ACS245S *UT54ACS245SE	Schmitt Trigger Octal Bus Transceivers w/Three-State Outputs
5962-96572 5962-96573 5962-96573	UT54ACS245 UT54ACTS245 *UT54ACTS245E	Octal Bus Transceivers with Three-State Outputs
5962-96578 5962-96578 5962-96579	UT54ACS273 * UT54ACS273E UT54ACTS273	Octal D Flip-Flops with Clear
5962-96588 5962-96589	UT54ACS373 UT54ACTS373	Octal Transparent Latches with Three-State Outputs
5962-96594 5962-96595 5962-96595	UT54ACS541 UT54ACTS541 *UT54ACTS541E	Octal Driver, with Three-State Output
5962-06239	UT54ACS630	EDAC



The MSI Logic Family is compatible to ACS and ACTS logic and has high speed, lower power consumption, 3- and 5-volt supply, and SEU threshold $80\,\text{MeV}$ - cm2/mg. We offer 14, 16, and 20 flatpack and 14, 16, and 20 DIP.



Multiplexers, Analog caes.com/HiRel	Asmonione. LVOMONE.	Smon mos me Smon one LVCM one	LVCMOSSD;	SOMO	0)8ita/10Scm	Ma: 1000 100 100 100 100 100 100 100 100 1	15/00/18EZ 100/18EZ	Catch-Up him	STATE SUPPLY SUP		so mo	J&C 1800 8
UT16MX110	•				*	300	62.3	110	4.5 to 5.5V	28 CFP	Q,V	5962-10233
UT16MX111					*	300	62.3	110	4.5 to 5.5V	28 CFP	Q,V	5962-10233
UT16MX112			-		*	300	62.3	110	4.5 to 5.5V	28 CFP	Q,V	5962-10233
UT16MX113	-				3.0 to 3.6	300	62.3	110	4.5 to 5.5V	28 CFP	Q,V	5962-10236
UT16MX114		-			3.0 to 3.6	300	62.3	110	4.5 to 5.5V	28 CFP	Q,V	5962-10236
UT16MX115			-		3.0 to 3.6	300	62.3	110	4.5 to 5.5V	28 CFP	Q,V	5962-10236
UT16MX116	-			-	3.0 to 5.5	300	62.3	110	4.5 to 5.5V	28 CFP	Q,V	5962-10237
UT16MX117			-		3.0 to 5.5	300	62.3	110	4.5 to 5.5V	28 CFP	Q,V	5962-10237

 $^{^*}$ Generated on chip. NOTE: RON < 300 Ω





Analog-to-Digital Converters caes.com/HiRel	Description	A 2006	\$00
RHD5950†*	The RHD5950 takes 16 analog sensor signals and using 4 address inputs and an enable input, selects one of the 16 analog inputs and converts the signal to 14 digital output bits. The 14-bit digital output has a tristate control allowing the connection of multiple RHD5950s. This provides a very high level of telemetry integration interfacing many sensor voltage readings to the digital processor data bus.	48 CQFP	5962R1220301KXC
RHD5958†*	The RHD5958 takes 8 analog sensor signals and using 3 address inputs and an enable input, selects one of the 8 analog inputs and converts the signal to 14 digital output bits. The 14-bit digital output has a tri-state control allowing the connection of multiple RHD5958s. This provides a very high level of telemetry integration interfacing many sensor voltage readings to the digital processor data bus.	40 CQFP	5962R1221101KXC

^{*} Multiplexed, 5V or 3.3V I/O † Contact factory for more information.





Digital-to-Analog Converters caes.com/HiRel	Description		*0Ws
RHD5930	Digital to Analog Converter, 11-bit, ladder output	16 SOIC	5962H1120801KXC
RHD5931	Digital to Analog Converter, 11-bit, buffered output	16 SOIC	5962H1120802KXC
RHD5932	Digital to Analog Converter, 14-bit, buffered output	20 SOIC	5962H1320101KXC

		ò	SS	Wene	tus. 17.	5 4	³ 5 કેડ				Dical)	Ø)	Win	Motor	isher	8/1	
Multiplexers, Analog caes.com/HiRel	2	Co Change	Kon .	Tanson Measurene	* A . O C C.	# COT-655 B/L	se rable se	77	1	5/0/6	4coss 7;	m''yoi''n Indu''	Mout B	Men Joseph	SEL: LET (15)	Sur China	*ONS
RHD5928*	8	8			1	1	+5V	GND	N/A	<750	<150	OV	+5V	1000	100	16 SOIC	5962H1220801KXC
MUX8520	16	16		-	1	1	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	56 CQFP	5962F0922901KXC
RHD5920*	16	16			1	1	+5V	GND	N/A	<750	<150	OV	+5V	1000	100	24 SOIC	5962H1024301KXC
RHD5921*Buffered	16	16			1	1	+5V	GND	N/A	N/A	<2000	OV	+5V	1000	100	24 SOIC	5962H1024302KXC
MUX8521	16		16	-	1	1	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	56 CQFP	5962F0922902KXC
MUX8522	32	32			2	2	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	56 CQFP	5962F0923101KXC
MUX8523	32	32		-	2	2	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	56 CQFP	5962F0923102KXC
RHD8544*	32	32			2	2	+5V	GND	N/A	<750	<150	OV	+5V	1000	100	56 CQFP	5962H1220901KXC
RHD8545 Buffered*	32	32			2	2	+5V	GND	N/A	N/A	<2000	OV	+5V	1000	100	56 CQFP	5962H1220902KXC
MUX8503	48	48		-	1	3	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	96 CQFP	5962F0323403KXC
RHD8543*	48	48			1	3	+5V	GND	N/A	<750	<150	OV	+5V	1000	100	96 CQFP	5962H1221002KXC
MUX8502	48		48	-	1	3	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	96 CQFP	5962F0323401KXC
MUX8506	48		48		1	3	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	96 CQFP	5962F0323402KXC
RHD8542*	48		48		1	3	+5V	GND	N/A	<750	<150	OV	+5V	1000	100	96 CQFP	5962H1221001KXC
MUX8500	64	32	32	-	2	4	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	96 CQFP	5962F0050201KXC
MUX8507	64	32	32		2	4	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	96 CQFP	5962F1021201KXC
RHD8540*	64	32	32		2	4	+5V	GND	N/A	<750	<150	OV	+5V	1000	100	96 CQFP	5962H1124001KXC
MUX8501	64	64		-	2	4	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	96 CQFP	5962F0050202KXC
MUX8509	64	64			2	4	+15V	-15V	+5V	<2000	<1500	-5V	+15V	300	120	96 CQFP	5962F1021202KXC
RHD8541*	64	64			2	4	+5V	GND	N/A	<750	<150	OV	+5V	1000	100	96 CQFP	5962H1124002KXC

^{*} Power Supply requirements: Only +5V and ground.







Op Amps caes.com/HiRel	Description		ss. *Ons
RHD5900 Quad Op Amp	Quad Operational Amplifier with rail-to-rail input and outputs for general purpose operational amplifier applications.	16 SOIC	5962H1024101KXC
RHD5901 Quad Op Amp	Quad Operational Amplifier configured with enable/disable control. Pairs of amplifiers are put in a power-down condition with their outputs in a high-impedance state.	16 SOIC	5962H1024102KXC
RHD5902 Quad Op Amp	Higher-speed version of RHD5901 providing wider bandwidth and faster slew rate.	16 SOIC	5962H1024103KXC

Comparators caes.com/HiRel	Description	A action	% / MS
RHD5910 Quad Comparator	Quad Comparator, High Speed, for operation with dynamic signals on either or both inputs. Comparison is continuous as the circuit functions as high gain open loop amplifier with a digital output.	16 SOIC	5962H1024201KXC
RHD5912 Quad Comparator	Quad Comparator with open drain outputs with Vol < 1.0 V with sink current 20 mA.	16 SOIC	5962H1024203KXC

Precision Current Source (PCS) caes.com/HiRel	Description	104/2	(Spery Soot)	3° / 8° / 8° / 8° / 8° / 8° / 8° / 8° /
PCS5035 Quintet Precision Current Source	Monolithic quintet (5) precision current sources (each at 80µA) designed for thermistor current monitor and resistive sensor applications. Built-in comparators and precision internal 2.0VDC reference further simplifies the application design.	100	18 FP	5962R0923401KXC
PCS5038 Octal Precision Current Source	The PCS5038 was designed to provide the flexibility needed to support a very wide range of resistive sensors. It contains eight precision current sources that can be set to source from 100uA to 2mA each with a single external resistor. Any number of the eight current source outputs can be tied together allowing the PCS5038 to drive multiple current source values.	100	40 CQFP	5962R1223201KXC



Precision References and Thermometers caes.com/HiRel	Description		S/W *
Precision References and Thermometers			
RHD5961	Precision Reference, 2.00V, Temperature Coefficient < 35 ppm/°C	SMD-0.5	5962H1422101KXC
RHD5964†	Precision Reference, 2.50V, Temperature Coefficient < 35 ppm/°C	SMD-0.5	5962-1422104KXC
RHD5962	$Thermometer, Buffered \ Output, Initial \ Accuracy: 1.00 \ V \pm 50 \ mV, Temperature \ Coefficient: 10 \ mV/^{\circ}C$	SMD-0.5	5962H1422102KXC
RHD5963	Integrated RHD5961 2.00V Precision Reference and RHD5962 Buffered Thermometer	SMD-5Pad	5962H1422103KYC

[†] Contact factory for more information.

RadHard-by-Design **Analog Function** Series

caes.com/HiRel

Single power supply operation: 5V Radiation performance:

Description

CMOS ELDRS Immune

re: CMOS ELDRS IIIIIIIII
Total dose > 100 krad(Si) to 1 Mrad(Si)
SEL Immune > 100 MeV-cm2/mg
Displacement Damage > 1014 neutrons/cm2



Quad Op Amps			
RHD5900	Quad Operational Amplifier with rail-to-rail inputs and outputs for general purpose operational amplifier applications.	16 SOIC	5962H1024101KXC
RHD5901	Quad Operational Amplifier configured with enable/disable control. Pairs of amplifiers are put in a power-down condition with their outputs in a high impedance state.	16 SOIC	5962H1024102KXC
RHD5902	Higher-speed version of RHD5901 providing wider bandwidth and faster slew rate.	16 SOIC	5962H1024103KXC
Quad Comparators			
RHD5910	Quad Comparator, High Speed, for operation with dynamic signals on either or both inputs. Comparison is continuous as the circuit functions as a high gain open loop amplifier with a digital output.	16 SOIC	5962H1024201KXC
RHD5912	Quad Comparator with open drain outputs.	16 SOIC	5962H1024203KXC
Analog Multiplexers			
RHD5920*	16:1 analog multiplexer. Channel selection is controlled by 4-bit binary addressing and an active low enable.	24 SOIC	5962H1024301KXC
RHD5921* Buffered	16:1 buffered output voltage multiplexer. Channel selection is controlled by 4-bit binary addressing and an active low enable. Multiplexed voltages are buffered by a unity gain rail-to-rail amplifier.	24 SOIC	5962H1024302KXC
RHD5928*	8:1 analog multiplexer. Channel selection is controlled by 3-bit binary addressing and an active low enable.	16 SOIC	5962H1220801KXC
RHD8541*	64 channels provided by four $16:\!1$ multiplexers. Two address busses A(0-3) and B(0-3) and four enable lines afford flexible organization.	96 CQFP	5962H1124002KXC
RHD8542*	48 channels channels are configured for Kelvin Measurement by connecting the addressed channel to the "Voltage" output and "Current" input pins. This enables selecting and reading a remote resistive sensor without the multiplexer on resistance being part of the measurement. Address bus A(0-3) and three enable lines afford flexible organization.	96 CQFP	5962H1221001KXC
RHD8543*	48 channels. Triple 16:1, common address inputs A(0-3), separate enable and output.	96 CQFP	5962H1221002KXC
RHD8544*	32 channels. Dual 16:1, separate address inputs A(0-3) and B(0-3), separate enable and output.	56 CQFP	5962H1220901KXC
RHD8545* Buffered	$Same\ configuration\ as\ RHD8544\ with\ multiplexed\ outputs\ buffered\ by\ a\ unity\ gain\ rail-to-rail\ amplifier.$	56 CQFP	5962H122O9O2KXC
Digital-to-Analog Converters			
RHD5930	Digital to Analog Converter, 11-bit, ladder output.	16 SOIC	5962H1120801KXC
RHD5931	Digital to Analog Converter, 11-bit, buffered output.	16 SOIC	5962H1120802KXC
RHD5932	Digital to Analog Converter, 14-bit, buffered output.	20 SOIC	5962H1320101KXC
Analog-to-Digital Converters			
RHD5950 Multiplexed†	16:1 Multiplexed, 14-bit Analog-to-Digital Converter takes 16 analog sensor signals and using 4-bit binary addressing and an enable input, selects one of the 16 analog inputs and converts the signal to 14 digital output bits. The 14-bit digital output has a tri-state control allowing the connection of multiple RHD5950s. This provides a very high level of telemetry integration interfacing many sensor voltage readings to the digital processor data bus.	48 CQFP	5962R1220301KXC
RHD5958 Multiplexed†	The RHD5958 takes 8 analog sensor signals and using 3 address inputs and an enable input, selects one of the 8 analog inputs and converts the signal to 14 digital output bits. The 14-bit digital output has a tri-state control allowing the connection of multiple RHD5958s. This provides a very high level of telemetry integration interfacing many sensor voltage readings to the digital processor data bus.	40 CQFP	5962R1221101KXC

^{*} Power Supply requirements: Only +5V and ground. † Contact factory for more information.

RadHard-by-Design
Analog Function
Series (continued)
cacc com/HiPol

Analog Function Series (continued) caes.com/HiRel	Description	School School	*Ons
Precision References and Thermometers			
RHD5961	Precision Reference, 2.00V, Temperature Coefficient < 35 ppm/°C	SMD-0.5	5962H1422101KXC
RHD5964†	Precision Reference, 2.50V, Temperature Coefficient < 35 ppm/°C	SMD-0.5	5962-1422104KXC
RHD5962	Thermometer, Buffered Output, Initial Accuracy: 1.00V \pm 50mV, Temperature Coefficient: 10 mV/ $^{\circ}$ C	SMD-0.5	5962H1422102KXC
RHD5963	Integrated RHD5961 2.50V Precision Reference and RHD5962 Buffered Thermometer	SMD-5Pad	5962H1422103KYC
Voltage Level Translators			
RHD5980	Octal Bidirectional Voltage Level Shifter	24 SOIC	5962H1222601KXC

 $[\]ensuremath{^{\dagger}}$ Contact factory for more information.

Pulse Width Modulators (PWM) caes.com/HiRel	Description	7049/	LET WOSOMOO(S)	(47.75) (47.00) (40.00)	Salamine Sal	*0vs
PWM5032 High-Speed PWM Controller	Optimized for power applications: Buck, Boost, Flyback, Forward and Center-Tapped Push-Pull converters. 1 V thru 12 V @ 1.0 A drive capability. Selectable $50\%/100\%$ duty cycle. Low power CMOS technology.	1000	20	100	24 SOIC	5962- 0625102KXC
PWM5034 High-Speed PWM Controller	Optimized for power applications: Buck, Boost, Flyback, Forward and Center-Tapped Push-Pull converters. 1 V thru 12 V @ 1.0 A drive capability. Selectable 50%/100% duty cycle. Low power CMOS technology with unformed leads.	1000	20	100	24 FP	5962- 0625102KYC



Resolver-to-Digital **Converter (RDC)** caes.com/HiRel

RDC5028 Resolver-to-Digital Converter







Bus Switch caes.com/HiRel	Description	10/4 BB 10/4		Ashistion (1)		om,	120 × 040
UT64BS1X433	Matrix-A 64-Channel 1:4 Bus Switch	3.3V	5	TID>300 krad(Si) SEL>100 MeV-cm2/mg	400 CLGA 400 CBGA 400 CCGA	Q,V	5962-15242
UT32BS1X833	Matrix-D 32-Channel 1:8 Bus Switch	3.3V	5	TID>300 krad(Si) SEL>100 MeV-cm2/mg	400 CLGA 400 CBGA 400 CCGA	Q,V	5962-15243
UT54BS32245	32-Bit 1:1 Bus Switch	3.3 & 5.0V	11 & 5	TID>300 krad(Si) SEL>100 MeV-cm2/mg	99 BGA	Q,V	5962-15241
UT54BS16210	20-Bit 1:1 Bus Switch	3.3 & 5.0V	11 & 5	TID>300 krad(Si) SEL>100 MeV-cm2/mg	48 Lead CFP	Q,V	5962-15245
UT54BS16245	16-Bit 1:1 Bus Switch	3.3 & 5.0V	11 & 5	TID>300 krad(Si) SEL>100 MeV-cm2/mg	48 Lead CFP	Q,V	5962-15240
UT54BS3245	8-Bit 1:1 Bus Switch	3.3 & 5.0V	11 & 5	TID>300 krad(Si) SEL>100 MeV-cm2/mg	20 Lead CFP	Q,V	5962-15244



Smart Power Switch Controller caes.com/HiRel	Description	(N. 88, W)	TO ARACK!	15 Jay 18 18 18 18 18 18 18 18 18 18 18 18 18		044	120 % NO %
UT36PFD103	Intelligent PowerMOSFET controller with load-side inrush current limiting, eFuse protection of current faults and telemetry through PMBus TM	8V - 36V	300	≤100	47-Lead CFP	Q, V	5962-2020
UT05PFD103	Intelligent PowerMOSFET controller with load-side inrush current limiting, eFuse protection of current faults and telemetry through PMBus TM	4.5V - 5.5V	300	≤100	47-Lead CFP	Q, V	Pending

Linear Adjustable Voltage Regulators caes.com/HiRel	704.	LDO Resulators	4 POUT VA	Relators Services	88° (V) ***	Sularive Nesative Voltage	Positive Court	Nent (4) but Chiefic	Total (A) whole	(Sherther)	24 80 52 6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Thu-Hou	41,0MO1.	* ONS
VRG8601	2		1	1.2 to 37	1	-1.2 to -27	1.5	1.5	100	TO-257	0.65x0.42x0.220		6	5962R0521901KXC
VRG8602	2		1	1.2 to 37	1	-1.2 to -27	1.5	1.5	100	TO-257	0.65x0.42x0.220		l 6	5962R0521901KYC
VRG8607	2		2	1.2 to 37			1.5		100	TO-257	0.65x0.42x0.220		6	5962R0521903KXC
VRG8608	2		2	1.2 to 37			1.5		100	TO-257	0.65x0.42x 0.220		l 6	5962R0521903KYC
VRG8609	2				2	-1.2 to -27		1.5	100	TO-257	0.65x0.42x0.220	-	6	5962R0521904KXC
VRG8610	2				2	-1.2 to -27		1.5	100	TO-257	0.65×0.42× 0.220	•	l 6	5962R0521904KYC
VRG8651	2	1.30	1	1.3 to 23	1	-2.5 to -25	1.0	3.0	100	TO-257	0.75×0.42×0.220		8	5962R0920101KUC
VRG8652	2	1.30	1	1.3 to 23	1	-2.5 to -25	1.0	3.0	100	TO-257	0.75×0.42×0.220		8	5962R0920101KZC
VRG8657	2	1.30	2	1.3 to 23			1.0		100	TO-257	0.65×0.42×0.220		6	5962R0920102KXC
VRG8658	2	1.30	2	1.3 to 23			1.0		100	TO-257	0.65x0.42x0.220		l 6	5962R0920102KYC
VRG8660	1		1	1.2 to 37			1.5		100	SMD-0.5	0.40x0.30x0.130		I 3	5962R0920601KXC
VRG8661	1				1	-1.2 to -27		1.5	100	SMD-0.5	0.40x0.30x0.130		I 3	5962R0920602KXC
VRG8662	1	1.30	1	1.3 to 23			1.0		100	SMD-0.5	0.40x0.30x0.130		I 3	5962R0920701KXC
VRG8663	1	1.05			1	-2.5 to -25		3.0	100	SMD	0.55x0.30x0.130		l 5	5962R0920702KYC
VRG8666	1	0.60	1	0.1 to 34			0.9		100	SMD	0.55x0.30x0.130		l 5	5962R1120501KYC
VRG8667	2	0.60	2	0.1 to 34			0.9		100	TO-257	0.75x0.42x0.220		8	5962R1320301KUC
VRG8668	2	0.60	2	0.1 to 34			0.9		100	TO-257	0.75×0.42×0.220		8	5962R1320301KZC
VRG8669	1	0.75	1	0.1 to 22			2.5		100	SMD	0.55x0.30x0.130		l 5	5962R1420101KYC
VRG8691	1	0.50	1	1.0 to 3.3			7.5		100	Power	0.90x1.00x0.220		12	5962R0923701KXC
VRG8692	1	0.50	1	1.0 to 3.3			7.5		100	Power	0.90x1.00x0.220		12	5962R0923701KYC
VRG8697	2	0.75	2	0.1 to 22			2.5		100	TO-257	0.75x0.42x0.220		8	5962R1420201KUC
VRG8698	2	0.75	2	0.1 to 22			2.5		100	TO-257	0.75x0.42x0.220		8	5962R1420201KZC







Voltage Supervisors caes.com/HiRel	7049/2	Solven See	40%	Over-Volts	16ct 1680 Watch	0000 July 1000	Total Drive	1020 - 020 - 100 -	Pochee	OMO	18) *OWS
UT04VS50P	4	3.3, 2.5, 1.8, 1.5, 1.2, 1.0	Yes	Yes	No	Yes	>300	< 110	28-lead CFP	Q,V	5962-13206
UT04VS33P	4	3.3, 2.5, 1.8, 1.5, 1.2, 1.0	Yes	Yes	No	Yes	>300	< 110	28-lead CFP	Q,V	5962-13206
UT01VS50L	1	1.25, VDD	No	No	Yes	No	> 300	< 110	8-lead CFP	Q,V	5962-11213
UT01VS50D	1	1.25, VDD	No	No	Yes	Yes	> 300	< 110	8-lead CFP	Q,V	5962-11213
UT01VS33L	1	0.6, VDD	No	No	Yes	No	> 300	< 110	8-lead CFP	Q,V	5962-11213
UT01VS33D	1	0.6, VDD	No	No	Yes	Yes	> 300	< 110	8-lead CFP	Q,V	5962-11213

Power Distribution Modules caes.com/power

Input Regulator Modules (IRM) Description caes.com/power PDM621100 100 Vdc Input Regulator Module 95-105 26-48 75 1.65"L x 1.31"W x 0.315"H PDM621070 70 Vdc Input Regulator Module 63-77 26-48 75 92 1.65"L x 1.31"W x 0.315"H PDM621028 26-48 28 Vdc Input Regulator Module 22-36 100 1.65"L x 1.31"W x 0.315"H







Isolated Point of Load Modules (iPOL) caes.com/power	Description	7,7,7		Nont	,	(Cur)	Fricience	
PDM613140	Vout = 1/40 x Vin iPOL	1/40	26-48	0.65-1.2	1.00	50.0	89	1.60"L x 1.21"W x 0.315"H
PDM613132	Vout = 1/32 x Vin iPOL	1/32	26-48	0.81-1.5	1.30	50.0	89	1.60"L x 1.21"W x 0.315"H
PDM613124	Vout = 1/24 x Vin iPOL	1/24	26-48	1.081-2.0	1.60	37.5	89	1.60"L x 1.21"W x 0.315"H
PDM612116	Vout = 1/16 x Vin iPOL	1/16	26-48	1.63-3.0	6.40	16.7	91	1.10"L x 1.31"W x 0.315"H
PDM612112	Vout = 1/12 x Vin iPOL	1/12	26-48	2.17-4.0	8.40	12.5	91	1.10"L × 1.31"W × 0.315"H
PDM612108	Vout = 1/8 x Vin iPOL	1/8	26-48	3.25-6.0	21.0	8.33	91	1.10"L × 1.31"W × 0.315"H
PDM612106	Vout = 1/6 x Vin iPOL	1/6	26-48	4.33-8.0	35.0	6.25	91	1.10"L × 1.31"W × 0.315"H
PDM612105	Vout = 1/5 x Vin iPOL	1/5	26-48	5.20-9.60	37.0	5.20	90	1.10"L × 1.31"W × 0.315"H
PDM612104	Vout = 1/4 x Vin iPOL	1/4	26-48	6.50-12.0	44.0	4.20	92	1.10"L × 1.31"W × 0.315"H
PDM612103	Vout = 1/3 x Vin iPOL	1/3	26-48	8.67-16.0	71.0	3.10	95	1.10"L x 1.31"W x 0.315"H
PDM612102	Vout = 1/2 x Vin iPOL	1/2	26-48	13.0-24.0	80.0	2.10	91	1.10"L x 1.31"W x 0.315"H
PDM612203	Vout = 2/3 x Vin iPOL	2/3	26-48	17.3-32.0	85.0	1.50	91	1.10"L x 1.31"W x 0.315"H
PDM612101	Vout = 1/1 x Vin iPOL	1/1	26-48	26.0-48.0	96.0	1.00	90	1.10"L x 1.31"W x 0.315"H

TID Tolerance (krad(Si)) = 100



- $\cdot\,6702\text{-EVAL}$ includes the 621100-7 IRM and 613140 IPOL
- \cdot 6703-EVAL includes the 621028-7 IRM and 613140 IPOL

Battery Power Management (BEU) for HiRel Applications

Battery Electronics Units caes.com/HiRel	Cells	Description	Size
	accurately ch converters the each cell is be Individual ce	lattery Electronics Units provide autonomous cell balancing for Lithium-Ion batteries. A series narge balanced so the battery can be utilized to its fullest capacity. The cell balancing circuitry nat tie the cells of the battery to a common share bus. Cell charge is distributed among the murought to the average charge of the other cells. Cell balancing can, therefore, be performed at all voltage monitors keep track of cells that may exceed charge limits. Precise voltage telemetrical features include reconditioning load control and cell bypass device drivers.	uses a set of bi-directional DC-DC litiple cells so that the charge of any state of charge of the battery.
BEU8635†	8, 12, 24	Balancing for 24-cell battery, with cell voltage monitoring and telemetry	11.50" L x 2.30" W x 5.25" H
BEU8636†	8, 12, 24	Balancing for 24-cell battery, with cell voltage monitoring and telemetry and cell bypass device drivers	11.50"L x 3.30"W x 5.25"H
BEU8637	8,12	Independent balancing for two 12-cell batteries or redundant balancing for a single 12-cell battery, with cell voltage monitoring and telemetry	11.50" L x 4.00" W x 5.25"H
BEU8638†	8,12	Independent balancing for two 12-cell batteries or redundant balancing for a single 12-cell battery, with cell voltage monitoring and telemetry, reconditioning load control and cell bypass device drivers	11.50" L x 5.20" W x 5.25" H
BEU8640	24	Dual redundant balancing for up to 24-cell battery, with cell voltage monitoring and telemetry, reconditioning load control and cell bypass device drivers	11.50" L x 5.30" W x 5.25" H
BEU8642-EVAL	8	Balancing for 8-cell battery, with cell voltage monitoring and telemetry, temperature monitoring, built-in test, RS-232 output for data logging, LCD display for cell voltage, temperature and status	12.00" L x 9.00" W x 2.65" H
BEU8642-EVAL1	8	Balancing for 8-cell battery, with cell voltage monitoring and telemetry, temperature monitoring, built-in test, RS-232 output for data logging, LCD display for cell voltage, temperature and status with external fuses	12.00" L x 9.00" W x 2.65" H

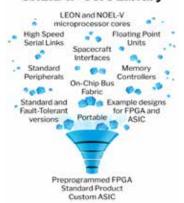
† Product in development. P



Battery Interface Electronic Assembly caes.com/HiRel	Cells	Description	Size
BIE8678	8 - 32	The Battery Interface Electronic (BIE) assembly provides an interface between a space vehicle electrical power system (EPS) and its' Lithium Ion batteries (comprised of 8 to 32 cells). The BIE provides real time battery status monitoring, telemetry and control, and insures safe battery operation throughout the mission life. It is fully space qualified and is designed to support a wide range of missions including LEO, MEO, GEO, HEO, interplanetary and manned flight. The BIE assembly includes three primary components: the Voltage/Temperature Monitoring Module (VTM), the Over Charge Protection Module (OCP), and the Battery Isolation Switch.	6.95" W x 11.71" L x 4.50" H

Licensable IP Cores and	
Processors caes.com/Gaisler	Description
LEON3 SPARC V8 Processor Core	The LEON3 is a synthesizable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The model is highly configurable, and particularly suitable for system-on-a-chip (SOC) designs. Delivery format is source code.
LEON3FT Fault-tolerant SPARC V8 Processor Core	The LEON3FT is a fault-tolerant version of the standard LEON3 SPARC V8 Processor. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.
LEON3FT for Microsemi Space- Grade FPGAs	The LEON3FT adapted for optimum performance using the Microsemi RTG4, RTAX, RTProASIC3 and RT PolarFire FPGAs. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.
LEON3FT for Xilinx FPGAs	The LEON3FT adapted for optimum performance using the Xilinx RT Kintex Ultrascale and Virtex-5QV FPGAs. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.
LEON3FT for NanoXplore	The LEON3FT adapted for optimum performance using the NanoXplore NG-Medium, NG-Larg, NG-Ultra, and NG-Ultra300 FPGAs. It has been designed for operation in the harsh space environment, and include functionality to detect and correct (SEU) errors in all on-chip RAM memories, Delivery format is encrypted VHDL.
LEON4 SPARC V8 Processor Core	The LEON4 is a synthesizable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The new 64/128 bit bus width architecture significantly improves performance over previous generations. The model is highly configurable, and particularly suitable for system-on-a-chip (SOC) designs. Delivery format is source code.
LEON4FT Fault-tolerant SPARC V8 Processor Core	The LEON4FT is a fault-tolerant version of the standard LEON4 SPARC V8 Processor. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.
LEON5 SPARC V8 Processor Core	The LEON5 is a high-performance dual issue (Superscalar) processor conforming to the 32-bit SPARC V8 RISC architecture with enhanced branch prediction. The model is highly configurable, and particularly suitable for system-on-a-chip (SOC) designs. Deliver format is source code for LEON5.
LEON5FT SPARC V8 Processor Core	The LEON5FT is a fault tolerant, high-performance dual issue (Superscalar processor conforming to the 32-bit SPARC V8 RISC architecture with enhanced branch prediction. The FT version has been designed for harsh space environments and includes functionality to detect and correct (SEU) errors in all on-chip RAM Memories. Unlike earlier generation LEONs, cache memory is protected by full SECDED code. Delivery format is encrypted VHDL for LEON5FT.
LEON5FT for Microsemi FPGAs	The LEON5FT adapted for optimum performance using Microsemi RT PolarFire and RTG4 FPGAs, designed for operation in space environments and delivered in encrypted VHDL.
LEON5FT for Xilinx FPGAs	The LEON5FT adapted for optimum performance using Xilinx RT Kintex Ultrascale FPGAs, designed for operation in space environments and delivered in encrypted VHDL.
LEON5FT for NanoXplore FPGAs	The LEON5FT adapted for optimum performance using the NanoXplore NG-Ultra and NG-Ultra300 FPGAs. It has been designed for operation in the harsh space environment, and include functionality to detect and correct (SEU) errors in all on-chip RAM memories/ Delivery format is encrypted VHDL.
NOEL-V RISC-V Microprocessor Core	The NOEL-V implements the RISC-V instruction set architecture. It is configurable to meet performance and area requirements and can be implemented as a 32-bit (RV32) or 64-bit (RV64) processor, which will allow for significant improvements versus the LEON processor both in terms of computational performance and software aspects. Leverage of RISC-V software and tool support in the commercial domain. Delivery format is source code for NOEL-V.
NOEL-V FT RISC-V Microprocessor Core	The NOEL-V implements a fault tolerant version of the RISC-V instruction set architecture. It is configurable to meet performance and area requirements and can be implemented as a 32-bit (RV32) or 64-bit (RV64) processor, which will allow for significant improvements versus the LEON processors both in terms of computational performance and software aspects. The FT version has been designed for harsh space environments and includes functionality to detect and correct (SEU) errors in all on-chip RAM Memories. The cache memory is protected by full SECDED code. Leverage of RISC-V software and tool support in commercial domain. Delivery format is encrypted VHDL for NOEL-V FT.
NOEL-V FT for Microsemi FPGA	The NOEL-V fault tolerant RISC-V processor is adapted for optimal performance using Microsemi RT PolarFire and RTG4 FPGAs, designed for operation in space environments and delivered in encrypted VHDL.
NOEL-V FT for Xilinx FPGAs	The NOEL-V fault tolerant RISC-V processor is adapted for optimal performance using Xilinx RT Kintex Ultrascale FPGAs, designed for operation in space environments and delivered in encrypted VHDL.
NOEL-V FT for NanoXplore FPGAs	The NOEL-V fault tolerant RISC-V processor is adapted for optimal performance using the NanoXplore NG-Ultra and NG-Ultra300 FPGAs. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.

GRLIB IP Core Library



Licensable IP Cores caes.com/Gaisler	Description
GRLIB - Portable IP library	The GRLIB IP Library is an integrated set of over 130 reusable IP cores, designed for system-on-chip (SOC) development. The IP cores are centered around the common AMBA 2.0 on-chip bus, and use a coherent method for simulation and synthesis. A unique plug & play method is used to configure and connect the IP cores without the need to modify any global resources. Delivery format is source code.
GRFPU - IEEE-754 Floating-Point Unit	The GRFPU is an IEEE-754 compliant floating-point unit, supporting both single and double precision operands. The advanced design combines high throughput with low latency, providing up to 250 MFLOPS on a 0.13µm ASIC process. Delivery format is encrypted VHDL. This IP is suitable for LEON3 and LEON4.
GRFPU Lite - IEEE-754 Floating-Point Unit	The GRFPU Lite is an IEEE-754 compliant floating-point unit, supporting both single and double precision operands. The lightweight, non-pipelined design makes it particularly suitable for FPGA technologies with limited logic resources. Delivery format is encrypted VHDL. This IP is suitable for LEON3 and LEON4.
GRFPU5 IP Core	The GRFPU is an IEEE-754 complant floating-point unit (FPU), supporting both single and double precision operands. The advanced design combines high throughput with low latency. Delivery format is encrypted VHDL.
GRFUPnv IP Core	The GRFPUnv is a high-preformance pipelined floating-point unit (FPU) for the RISC-V architecture. The NOEL-V floating-point unit supports 32 and 64 bit floating-point operations, according to the RISC-V standard which in turn is based on IEEE-754-2008. Delivery format is encrypted VHDL.
GRPCI2 - Master/Target PCI Bridge	The GRPCI2 provides a 32-bit master/target interface for AMBA AHB-2.0 systems. It includes parameterizable FIFOs for both master and target operation, and can optionally be provided with an independent DMA engine. Delivery format is source code.
GR1553B	The GR1553B core implements the MIL-STD-1553B (Notice 2) data bus protocol, with ability to serve as Bus Controller (BC), Remote Terminal (RT) or Bus Monitor (BM). The core is connected to the MIL-STD-1553B bus via a dual transceiver interface (txP/N/en, rxP/N/en). On the system side, the core connects to the AMBA bus as an AHB master for DMA transfers and an APB slave for register access. The core uses a separate 20 MHz clock for the MIL-STD-1553B codec, and runs at any AMBA clock frequency from 10 MHz and upwards. Delivery format is encrypted VHDL.
GRSPW2 - SpaceWire Link	The GRSPW2 implements a SpaceWire Link with RMAP support and AMBA host interface. The core implements the SpaceWire standard with the protocol identification extension (ECSS-E-50-12 part 2) and RMAP protocol. Receive and transmit data is autonomously transferred between the SpaceWire Codec and the AMBA AHB bus using DMA. Delivery format is encrypted VHDL.
GRSPWROUTER - SpaceWire Router	The SpaceWire router core implements a SpaceWire router as defined in the ECSS-E-ST-50-12C standard. It supports from 0 to 31 ports (excluding the mandatory configuration port) which can be individually configured to be external SpaceWire links, FIFO ports or AHB ports. The AHB ports are limited to a maximum of 16 in a single router. Delivery format is encrypted VHDL.
GRSPFI IP Core	The GRSPFI provides and interface between the system bus (such as AHB or AXI) and a SpaceFibre network. It features a single-lane implementation of a SpaceFibre node designed in accordance to the SpaceFibre specification ECSS-E-ST-50-11C, as well as a flexible DMA engine with a programmable number of independent DMA channels. Delivery format is encrypted VHDL.
GRETH/GRETH_GBIT - 10/100/1000 Mbit Ethernet MAC	The GRETH_GBIT implements a 10/100/1000 Mbit/s Ethernet Media Access Controller (MAC) with AMBA host interface. The core implements the 802.3-2002 Ethernet standard. Receive and transmit data is autonomously transferred between the Ethernet MAC and the AMBA AHB bus using DMA. Delivery format is source code.
GRUSBHC - USB 2.0 Host Controller	The USB 2.0 Host Controller provides a link between the AMBA on-chip bus and the Universal Serial Bus (USB). The host controller supports High-Full- and Low-Speed USB traffic. USB 2.0 High-Speed functionality is supplied by an enhanced host controller implementing the Enhanced Host Controller Interface (EHCI). Full- and Low-Speed functionality (USB 2.0 and USB 1.1) is supplied by one or more companion controllers implementing the Universal Host Controller Interface (UHCI). Delivery format is source code.
GRUSBDC - USB 2.0 Device Controller	The USB 2.0 Device Controller provides an interface between an USB 2.0 bus and an AMBA-AHB bus. The core is used for implementing USB 2.0 functions providing access to the USB through either an AHB slave or an AHB master interface. The master interface is capable of higher bandwidths but is more complex and requires external memory. The slave interface is simpler and does not require external memory but is more bandwidth limited. UTMI, UTMI+ and ULPI PHYs are supported. Delivery format is source code.
GRCAN - CAN 2.0 Controller	The GRCAN provides a CAN 2.0 controller for AMBA AHB-2.0 systems. The CAN controller supports transmission and reception of sets of messages by use of circular buffers located in memory external to the core. Transmit and receive buffers are organized separately. Reception and transmission of sets of messages can be ongoing simultaneously. Delivery format is source code.
GRCANFD - CAN FD Controller	The GRCANFD is a CAN controller that supports CAN 2.0B and CAN FD. The CAN controller supports transmission and reception of sets of messages by use of circular buffers located in memory external to the core, which are accessed through an AMBA 2.0 AHB interface or an AXI4 interface. Transmit and receive buffers are organized separately. Reception and transmission of sets of messages can be ongoing simultaneously. Delivery format is source code.
I2CMST - Inter IC Bus Interface	The I2C bus is a simple 2-wire serial multi-master bus with collision detection and arbitration. The bus consists of a serial data line (SDA) and a serial clock line (SCL). Both the master and a slave cores are provided. Delivery format is source code.
SPICTRL - Serial Peripheral Interface	The core provides a link between the AMBA APB bus and the Serial Peripheral Interface (SPI) bus. Through registers mapped into APB address space, the core can be configured to work either as a master or a slave. Delivery format is source code.
GRAES/GRECC - Crypotography Cores	The GRAES - Advanced Encryption Standard (AES) cryptography and the GRECC - Elliptic Curve Cryptography (ECC) cryptography cores combine high throughput performance with seamless integration with the LEON3 32-bit SPARC processor core. Delivery format is source code.
CCSDS/ECSS Spacecraft Data Handling	The CCSDS/ECSS Spacecraft Data Handling IP cores represent a collection of cores that have been developed specifically for the space sector. These IP cores implement functions commonly used in spacecraft data handling and management systems. Delivery format is source code.

Please visit www.caes.com/Gaisler for a full list of available IP cores.

Licensable IP Cores caes.com/Gaisler	Description
GRDMAC2	The GRDMAC is a flexible Direct Memory Access controller with an integrated AHB/APB bridge. Access to APB peripherals is performed bypassing the processor AHB bus, consequently reducing AHB bus load and avoiding congestion. Also has AES encryption. Delivery format is source code.
L2C - Level 2 Cache Controller	The Level 2 Cache Controller instantiates EDAC protected cache memory in configurations of up to four cache ways and way sizes of up to 512 KiB. The Level 2 Cache acts as an AHB to AHB bridge between the processor bus and the memory bus, both configurable to a data width of up to 128 bit. Delivery format is source code.
FTADDR IP Core	The FTADDR is a DDR2/DDR3 controller with an EDAC providing correction of two independent 8-bit lanes. FTADDR provides a SEFI detection mechanism. On the memory side, it presents a DFI interface for connection to an on-chip physical layer (PHY) that manages the low-level timing and data recovery and then provides the I./O buffers. Delivery format is encrypted VHDL.
FT NAND Controller	Advanced NAND Flash controller IP core with EDAC and SEFI detection and handling. In development at the time of printing this catalog; please contact factory for updated information.
GRSCRUB	The GRSCRUB is an external FPGA scrubber controller responsible for programming and monitoring the FPGA configuration memory with support for the Kintex UltraScale and Virtex-5 Xilinx FPGA families. Delivery format is source code.
MEMSCRUB	The Memory Scrubber can be programmed to read through a memory area and write back the contents whenever a correctable error is detected. It monitors an AMBA AHB bus for accesses triggering an error response, as well as correctable error signals from cores containing EDAC, and triggers an interrupt in case of errors. It can be programmed to initialize a memory area to known values. Delivery format is source code.

Co	m	po	ne	m	s
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Description

GR718B 18-port SpaceWire Router	The GR718B is a radiation tolerant 18-port SpaceWire Router with integrated on-chip LVDS on 16 ports and 2 ports with LVTTL for use with off-chip LVDS transceivers. All SpaceWire links operate at up to 200 Mbit/s. The fault tolerant design of the router in combination with the radiation tolerant technology provides outstanding immunity to radiation effects. See page 8 for details.
GR712RC dual-core LEON3FT processor	The GR712RC is an implementation of the dual-core LEON3FT SPARC V8 processor using RadSafeTM technology. The fault tolerant design of the processor in combination with the radiation tolerant technology provides outstanding immunity to radiation effects. See page 4 for details.
GR740 quad-core LEON4FT processor	The GR740 is an implementation of the quad-core LEON4FT SPARC V8 microprocessor. The fault tolerant design of the processor in combination with the radiation tolerant technology provides outstanding immunity to radiation effects. See page 4 for details.
GR716A Microcontroller	The GR716A features a 50MHz fault-tolerant, single core LEON3 SPARC V8, 32-bit instruction set processor with support for LEON-REX 16-bit compressed mode, with various communication interfaces (SpaceWire, CAN 2.0B, MIL-STD-1553, SPI, I2C) and on-chip ADC (2xADC, 11-bit resolution), DAC (12-bit resolution at 3Mbps, 4 channels), programmable PWM, on-chip temperature sensor, Power-on-Reset, Oscillator Brown-out detections, LVDS transceivers, and on-chip LDO and integrated PLL. This microcontroller is ideally suited for space and other high-rel applications, such as satellite supervision, monitoring and distributed control.
GR716B Microcontroller	The GR716B is an enhanced version of the GR716A microcontroller with the same features in the same package, but running at twice the speed (100 MHz), with support for SRAM & SPI (on memory interface). Additional features include support for 4-byte Address Mode on the external SPI memory interface, hardware FPGA programming and scrubber, 2-port SpaceWire router, 2xCAN-FD (CANopen support for remote boot), enhanced PWM interface, 10/100 Ethernet, Programmable Enhanced DMA, 4xADC 13-bit resolution, LVDS with cold spare & fail safe support, and 20x Analog comparator. This product is in development at the time of the printing; please contact factory for availability See above for application examples.

caes.com/Gaisler	Description
GRMON	GRMON is a hardware debug monitor with a graphical user interface (GUI) for SPARC/LEON and RISC-V/NOEL-V processors. It communicates with the on-chip Debug Support Unit (DSU) and allows non-intrusive debugging of the complete target system. GRMON can be used for automatic board testing using Tcl scripts.
TSIM ERC32/LEON Simulator	TSIM is an instruction set simulator capable of emulating ERC32- and LEON-based computer systems, developed for near-real time performance. The simulator enables development and debugging of target applications before real hardware is available, thereby shortening the product development cycle. TSIM can be extended by user modules and operated by a library API, allowing for integration of the simulator into a larger simulation framework.

Compilers and Operating Systems

caes.com/Gaisler

Description

Bare-C Cross-Compiler System
(BCC and BCC2)

BCC is open source and royalty-free. It includes: GNU C/C++ Compiler with binutils, Simple bare-C runtime with interrupt support and GNU gdb for C/C++ source level debugging. BCC2 includes the LLVM compiler with LEON-REX 16-bit instruction set support.

RTEMS Cross-Compiler System (RCC)

RCC is open source and royalty-free. It includes: GNU C/C++ Compiler with binutils, RTEMS real-time kernel versions 4.10 and 5, network and file system support, GNU gdb for C/C++ source level debugging. RTEMS 5 supports Symmetric Multi-processing (SMP) in addition to Asymmetrical Multi-processing (AMP).

Buildroot Embedded Linux for LFON

Linux is open source and royalty-free. The LEON Linux development environment includes Linux kernel, C Library, compiler tools and the buildroot distribution. Buildroot is a full source embedded Linux distribution containing libraries and applications for rapid development of custom embedded Linux systems. Support for V8 mul/div instructions and Floating Point Unit (FPU) is included. There is Symmetric Multiprocessing (SMP) support for LEON systems with multiple processors.

VxWorks 6.9 and 7 port and BSP for LEON

The VxWorks-6.9/7-LEON are ports of the Wind River VxWorks 6.X operating system versions 6.9 and 7 to the LEON processor. A BSP and drivers for all standard on-chip peripherals are included. Development can be done on Linux or Windows hosts. The port and BSP are provided in full source code with example projects supplied. Requires source code license for VxWorks. BSPs support the UT699, UT700, GR712RC and GR740 devices.

Zephyr RTOS port and BSPs

Zephyr RTOS is an open-source and royalty-free real-time operating system. It is highly configurable with a tiny footprint, providing RTOS solution even for systems with smaller memory. BSPs and certain GRLIB device drivers are available.

GRBOOT Bootloader

GRBOOT is a flight software boot loader. It provides initialization, self-tests, and application loading functionality for payload and on-board computers. Compatible with the ESA SAVOIR Flight Computer Initialization sequence (SAVOIR-GS-002) specification and developed in accordance with the European software engineering standards ECSS-E-ST-40C and ECSS-Q-ST-80C, criticality category B., BSPs are available for GR740, GR712RC and UT700 and is capable of booting the supported operating systems.

GRBOOT-STANDBY Bootloader

The GRBOOT-STANDBY package includes the GRBOOT boot loader and an additional maintenance mode software compatible with the SAVIOR-GS-002 Standby functionality. The software maintenance mode is executed as part of the boot loader and allows for application uploading and patching and diagnosis remotely controlled over the SpaceWire PUS (ECSS-E-ST-70-41C) protocol. Developed in accordance with the European software engineering standards ECSS-E-ST-40C and ECSS-Q-ST-80C criticality category B. BSPs are available for the GR740 and GR712RC.

NOFL-V various

The NOEL-V processor implements the RISC-V ISA which means that compilers and kernels for RISC-V can be used with NOEL-V (kernels will need a NOEL-V BSP). To simplify software development, there are several prebuilt toolchains available. Currently, the NOEL-V processor is supported by pre-built bare-metal, RTEMS and Linux toochains, and a Zephyr RTOS BSP is available. VxWorks 7 BSP for NOEL-V is available under commercial license. Leverage of RISC-V software and tool support in the commercial domain.

Test Equipment

caes.com/Gaisler

Description

GRESB SpaceWire/Ethernet Bridge

The GRESB bridge facilitates rapid development and testing of equipment with SpaceWire interfaces. It provides three bi-directional SpaceWire links with a maximum bit rate of 100 Mbit/s and six "virtual" links that are interfaced through TCP sockets. Each SpaceWire link can be individually configured with respect to the transmission bit rate. The GRESB also supports one CAN 2.0B interface.

Telemetry and Telecommand FGSF

The CCSDS / ECSS Telemetry and Telecommand EGSE (Electrical Ground Support Equipment) provides the necessary means for communicating with the on-board space segment. It has been designed to support satellite integration and test activities, on-board space segment development, ground segment applications, etc.





GR-GR740-BOX

Boards caes.com/Gaisler	Description		
GR-CPCI-GR740	MHz. The board is cPCI form factor and dual Ethernet, 8 SpaceWire ports capab	DN4FT quad-core SPARC V8 microprocessor capable of running at a system clock span also be used in a standalone bench-top configuration. The board supports 32-bit, e of running up to 200Mbit/s, on-board FLASH, SDRAM and a socket for a PROM de econdary GPIO are available through an accessory board. A USB debug port is provid	/33MHz PCI, vice. 2 CAN
GR-VPX-GR740 Development Board	GR740 quad-core 32-bit fault-tolerant GR-VPX-GR740 board comes in a 6U VF (including mezzanine board). The board tionality. The board is equipped with on-	I has been designed to support the development and fast prototyping of systems ba R740 LEON4FT SPARC V8 processor supporting OpenVPX and SpaceVPX environ X format (233.5 mm x 160 mm) and is intended for use in OpenVPX chassis occupying an also be used in stand-alone operation with a single 12V supply, in this case with line board memories for boot and application storage, and an SODIMM for SDRAM. The first and LED indicators, whereas the rear connectors are intended for OpenVPX/Space	ments. The ng a 1" slot nited VPX func- ront panel
GR-GR740-BOX	and two Ethernet interfaces, as well as pand Break switches, DIP switches for bo	n allows convenient bench-top use of the unit. The front panel provides access to eig in headers, LEDs and DIP switches for 16 GPIO. The mini-USB FTDI JTAG debug con otstrap selection and further status LEDs are located at the front-panel as well. The be dundant MIL-STD-1553, one SPI and two RS-232 UART interfaces. Power is suppli- panel.	nector, Reset back panel hosts
GR-CPCI-XC7K	six SpaceWire MDM9 connectors, redur	CI board, especially developed for LEON development, with on-board DDR3 memory, dant MIL-STD-1553B and CAN 2.0B connectors, two E-SATA GTX connectors, USB asion connectors. The board is capable of operating stand-alone, as a Compact-PCI process.	and Ethernet
GR712RC-BOARD		core LEON3FT SPARC V8 microprocessor capable of running at a system clock spec ire ports capable of running up to 200Mbit/s, 2 CAN ports, dual 1553, SPI, I2C, on-bo provided.	
GR-CPCI-GR716-DEV GR716	faces include SpaceWire (LVDS), GPIO (6	GR716-board to be useful. It is a 6U cPCI format board with 2 slots wide front panel. F 44 pins), and FTDI (USB interface). The board has an expansion slot which can be used 1553 and SPI or for other user-defined functions. Clocks for the system, SpaceWire,	d with the pro-
GR716 MINI	rapid evaluation of the microcontroller a	nicrocontroller. The board has small dimensions (50mm x 35mm, 37.5% of a credit c chitecture. The board offers SPI Flash PROM (32 MiB) and SRAM (2 MiB) memories an be borrowed free of charge and can be used with the GRMON3 evaluation version	and a USB inter-
GR716-BOARD	an SPI Flash ROM (32MB) and a socket of	13 microcontroller. The board has a small form factor (80 x 100 mm) and supports UA scillator. Moreover, the PCI-104 headers (2x 64 pins) provide an interface to user-def to the GR-CPCI-GR716-DEV Interface Board.	
GR718B-BOARD	standalone bench-top configuration. The	on tolerant 18-port SpaceWire router. The board is 6U cPCI form factor and can also board supports 18 SpaceWire ports capable of running up to 200Mbit/s through frots are driven by on-board LVDS transceivers, the remaining 16 ports are driven by that is provided.	nt-panel
GR-PCI-XC5V	PCI format plug in board, with on-board tors. The Mezzanine and accessory boar	oard. The GR-PCI-XC5V is a LEON PCI Development board, with a Xilinx Virtex 5, XC 50-DIMM, SRAM, FLASH, GBit Ethernet, USB 2.0, DSU UART, user and memory expads for our CPCI boards can be used with this board. The standard version of this boar package. However, this board can also be equipped with the larger XC5VLX85 and L	nsion connec- d is equipped
GR-CPCIS-XCKU	plane format, and can be used stand alor ceptible to single event upsets (bit flips) Ultrascale FPGA, in a XCKU060 sized de have the same footprint. The GR-CPCIS features include an FPGA to DDR3 SDR/	ent board for XCKU060 & others. The GR-CPCIS-XCKU is a 1 slot, 6U high board with the on the bench top or installed in a CPCI-Serial rack. The SRAM-based FPGA on the in its configuration memory when used in harsh environments. This board implement vice 1517 ball-grid-array package and is compatible with larger devices of the same size XCKU board features an optional GR716 microcontroller acting as a supervisor for the Min via 2 SODIMM connectors, SPI Flash for FPGA configuration, FMC mezzanine exporter (8), SpaceWire (8), CAN, SPGIO & I2C and front panel interfaces of RJ45 (2), eSATLVDS (2), USB (2), JTAG & UARTS (3).	board is sus- is a large Xilinx series which he FPGA. Key pansion connec-
GR-VPX-XCKU060	ment board with a Xilinx Kintex Ultrascal FPGA to DDR3 SDRAM via 2 SODIMM c	ent board. The GR-VPX-XCKU060 is a OpenVPX compatible, 6U format, Payload pro e 060 FPGA and a GR716 microcontroller acting as a supervisor for the FPGA. Key for connectors, SPI Flash for FPGA configuration, FMC mezzanine expansion connectors paceFibre (data), VPX, utility management and front panel interfaces of SpaceFibre (to FMC.	eatures include (3), with back-
GR-CPCI-XC4V		ormat plug in board, especially developed for LEON development, with on-board SO- pansion connectors. The board is capable of operating stand-alone, as a Compact-P(





RadHard Digital ASIC Products caes.com/ASICS	Description Radical Asic Class Y
UT90nHBD - 90nm	Hardened-by-Design performance ASICs. Up to 50 M usable gates; toggle rates up to 5 GHz; +2.5 V/1.8 V I/O and +1.0 V core CMOS processed in commercial fab; RadHard from 100 to 300 krad(Si). QML V & Q, Class Y Flip-Chip - Configurable High Speed serial I/O supports SerDes, Rapid I/O and XAUI standards, 3.125 Gbps - State of the Art Trusted On shore fab - Ready for Design starts - RadHard Library available now! - QML Q and V Qualified, Class Y pending
UT130nHBD - 130nm	Ultra-low-power ASICs. Up to 15 M usable gates; toggle rates up to 4 GHz; +3.3 V/2.5 V/1.8 V I/O and +1.2 V core operation; CMOS processed in commercial fab; RadHard from 100 to 300 krad(Si). Class S, Wire Bond and Flip-Chip - SoC Platform design re-use with Leon SPARC V8 Processor-based standard products - Proven IP from Gaisler and CAES - FPGA development boards for prototyping - Highest density silicon for cost effective unit prices
UT0.25μHBD - 0.25μm	Up to 3.0 M usable gates; toggle rates > 1 GHz; single +3.3 V supply or +3.3 V I/O and +2.5 V core operation; CMOS processed in commercial fab; RadHard from 100 krad(Si) to 1E6 rads(Si). QML V & Q. - Bigger FPGA conversions - 5 V tolerant inputs - RadHard-by-Design - Cost effective NRE
UT0.6µCRH - 0.6µm	500 K usable gates; clock rates > 150 MHz; +5 V and +3.3 V operation; CMOS processed in commercial fab; RadHard from 100 to 300 krad(Si). QML V & Q. - Ideal for small FPGA and CPLD conversions - Lowest NRE - Fully Trusted supply chain - True 5 V drive capability - RadHard process
ASIC Design System	Supports design signoff in Synopsys and Mentor tools, and tools using VHDL and Verilog languages.
FPGA to ASIC Conversions	Convert RadHard (or non-RadHard) FPGAs (Field Programmable Gate Arrays) to high reliability RadHard ASICs.
Category 1A Trusted	Design, Assembly, and Backend Screening Services

RadHard Mixed-Signal ASIC Products caes.com/ASICS

Description

UT0.18µCRH-0.18µm	-1.8, 3.3 and 5.0 V Digital Core and/or I/O supplies - Substrate Isolated: Bipolar supplies from ±0.9 V to ±2.5 V - RadHard from 100 krad(Si) to 1 Mrad(Si), Latch-Up Immune > 110 MeV cm2/mg - Commercial, Hi-Rel, QML pending - 8 M gates with toggle rates up to 2.4 GHz - Extensive analog IP including 8-bit to 21-bit ADCs, DACs, op-amps, prog. filters, bandgaps, switched-cap circuits, voltage regulators, oscillators, level translators, CAES proprietary RadHard One-Time Electrically Programmable Metal Fuse NV Memory
UT0.35μCRH-0.35μm	- 3.3 and 5.0 V Digital Core and/or I/O supplies - Substrate Isolated: Bipolar supplies from ±1.65 V to ±20 V - Up to 40 V HV transistors - RadHard from 100 to 300 krad(Si), Latch-Up Immune > 110 MeV cm2/mg - Commercial, Hi-Rel, QML Q&V - 1.5 M gates with toggle rates up to 375 MHz - Extensive analog IP including 8-bit to 21-bit ADCs, DACs, op-amps, prog. filters, bandgaps, switched-cap circuits, voltage regulators, low RDS(on) switches, oscillators, level translators, CAES proprietary RadHard One-Time Electrically Programmable Metal Fuse NV Memory
UT0.6µCRH-0.6µm	- 3.3 and 5.0 V Digital Core and/or I/O supplies - Up to 20 V HV transistors - RadHard from 100 to 300 krad(Si), Latch-Up Immune > 110 MeV cm2/mg - QML Q&V - 500 K gates with toggle rates up to 215 MHz Extensive analog IP including bandgaps, op-amps, ADCs, DACs, oscillators, level-translators
ASIC Design System	Full custom design to customer performance specification and/or supports design signoff in Synopsys/Mentor tools, and tools using VHDL, Verilog languages.

Licensable IP Cores and Processors

LEON4FT Fault-tolerant SPARC V8

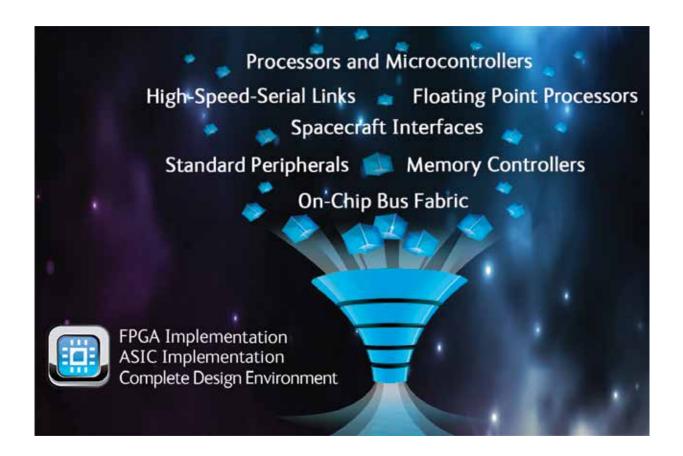
Processor Core

caes.com/Gaisler

Description

LEON3 SPARC V8 Processor Core	The LEON3 is a synthesizable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The model is highly configurable, and particularly suitable for system-on-a-chip (SOC) designs. Delivery format is source code.
LEON3FT Fault-tolerant SPARC V8 Processor Core	The LEON3FT is a fault-tolerant version of the standard LEON3 SPARC V8 Processor. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.
LEON3FT for Microsemi Space- Grade FPGAs	The LEON3FT adapted for optimum performance using the Microsemi RTG4, RTAX and RT ProASIC3 FPGAs. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.
LEON3FT for Xilinx Virtex-5QV FPGAs	The LEON3FT adapted for optimum performance using the Xilinx Virtex-5QV FPGAs. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.
LEON4 SPARC V8 Processor Core	The LEON4 is a synthesisable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The new 64/128 bit bus width architecture significantly improves performance over previous generations. The model is highly configurable, and particularly suitable for system-on-a-chip (SOC) designs. Delivery format is source code.

The LEON4FT is a fault-tolerant version of the standard LEON4 SPARC V8 Processor. It has been designed for operation in the harsh space environment, and includes functionality to detect and correct (SEU) errors in all on-chip RAM memories. Delivery format is encrypted VHDL.



Circuit Card Assembly caes.com/CCA

The Circuit Card Assembly (CCA) capability consists of assembly, test and conformal coat in a high-mix/low-to-medium volume operation. Our process equipment and test capabilities provide for state-of-the-art manufacturing and are ISO 9001 and AS-9100 approved. We provide full turnkey or consignment sub-contract assembly services for high-reliability products including J-STD-001 and NASA 8739. We combine best commercial practices of circuit card assembly with our radiation-hardened integrated circuits to provide CCA solutions for the commercial space industry including a long history of installing Column

Grid and other unique assembly technologies. CAES works with our customers to develop and qualify unique assembly processes. We utilize 2D real-time X-rays to inspect hidden or critical assembly inspection concerns. Our CCAs are manufactured for space, military, and commercial programs where quality and process control are essential for mission success. Our new automated circuit card assembly line to help assemble your high volumes - view our video at caes.com/ems.

Advantages

High-reliability standards

Board layout

Supplier and BOM management

Access to CAES Standard Products and RadHard ASICs

Flown on commercial aircraft and commercial/military satellites

CCA Services

- · Quick turn assembly
- Material management
- · Flying probe testing
- · Board layout
- · Dock-to-stock with CAES ICs
- SMT, through-hole, test and coat
- Customer-specific processes

Production Services

- Build to print
- Prototype
- Engineering
- Oualification
- Very low to moderate production
- Quick turn from receipt of components and documents

Material Management

- Full turnkey or consigned material acquisition
- Supplier management
- · BOM management
- · Value-added component screening

IC Screening and Value-Added Capabilities

- PIND, RLAT, DPA, fine and gross leak
- · Packaging, electrical testing, tinning, forming, and programming

Microwave Filters caes.com.com/EMS

The scope of the capabilities include:

- Full Turn-Key Capability. Design, assembly and test of single or multiplexer cavity type filters for space application
- Full functional testing to customer specification, to include passive intermodulation and High Power testing in a thermal vacuum chamber, while monitoring for any multipaction events.
- Legacy: GPSII and GPSIII SV1-SV9 Diplexers and Triplexers and many

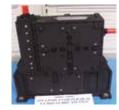




























Custom Hybrid, MCM, Module, Box Assembly and Testing Services caes.com.com/EMS

- · Space & MIL Qualified Assembly Services Certified Class K per MIL-PRF-38534
- · Vertically Integrated Die to Box Facility
- · DoD Microelectronics Trusted Source, Category 1A
- · Quick turn capable
- ISO 9001 and AS9100:2004 certified
- · Element evaluation and component screening

- Class 10,000 clean room for thick film substrate manufacturing
- Class 100,000 clean room for hybrid, SMT and box assembly
- · High Reliability Chip on Board Design & Manufacturing Services
- Full turnkey "Design to Spec" services for SMT Assemblies & Boxes
- RF Microwave Services for High Volume Phased Array Antennas





Trusted Accreditation caes.com.com/EMS

CAES Colorado Springs received Category 1A Trusted Accreditation by the Defense Microelectronics Activity as a Microelectronics Trusted Source for DoD and all other U.S. government users. The scope of the accreditation includes:

- Design Services
- · Aggregation Services
- Broker Services
- · Packaging and Assembly Services
- Test Services

Aeroflex Plainview received Category 1A Trusted Accreditation in 2010. Their scope includes:

· Multi-Chip Module and Hybrid Microcircuit Packaging and Assembly

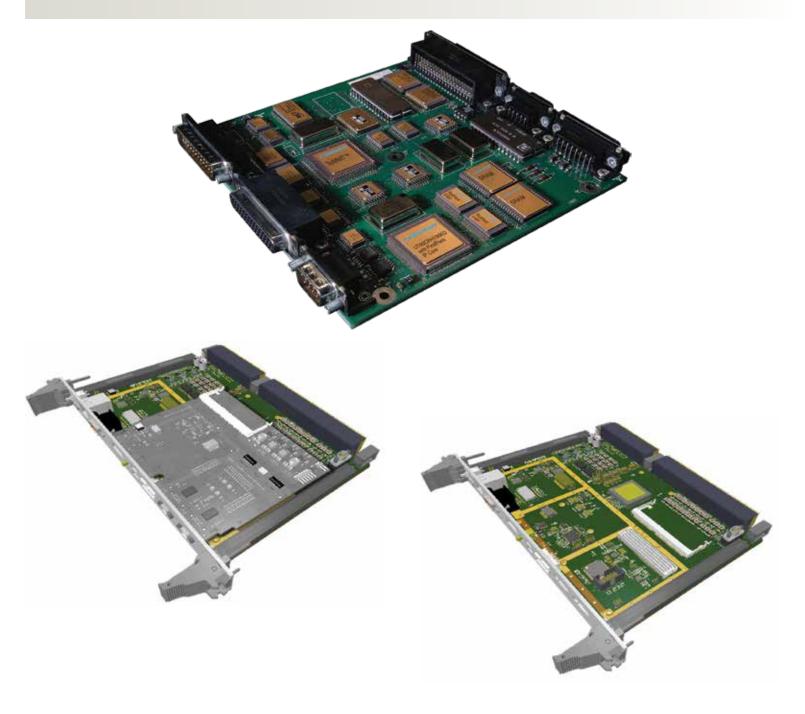
Single Board Computers caes.com.com/HiRel

Custom SBC Services - the scope of our capabilities include:

- Made-to-order SBCs
- Custom SBC module design (PCB design and layout, components circuit design, timing closure, form factor and mechanical casing/ shielding)
- Custom test solution for qualification and volume production
- Quick-turn Engineering Design Units (EDU) using lower cost HiRel or QCOTS components.
- Customer specified HiRel or Space grade qualification

Standard SBC Modification

- Customer system tuning and adaptation
- System Clock Frequency tuning and Power Management
- · Memory capacity customization



CAES Advanced Packaging Solutions caes.com/EMS

CAES offers advanced integrated circuit (IC) packaging, modelling and testing solutions for third-party ASIC and commercially-sourced die where the highest levels of reliability and performance are required along with stringent requirements in the areas of size, form-factor, power and thermal management. Building on a heritage of providing custom package solutions for the most demanding aerospace, defense, and medical IC products developed at CAES, we have a proven capability to identify, select, and design a solution tailored to the unique requirements of your mission. Our flexible engagement model allows us to support a range of services from rapid prototyping of a small number of die for validation and characterization to full volume production in our DMEA accredited trusted facility.

Numerous package technology and process flow options are available: ranging from ceramic QML to organic commercial. System in Package (SiP) solutions leveraging 2.1D technology to multiple die in a single package are available to enable smaller footprints, increased performance and the integration of die fabricated in different process technologies or wafer types.

A full suite of electrical, thermal, and mechanical modeling tools are used throughout the design process to ensure compliance with critical design points and constraints.

Package Technology Overview

- Commercial Organic Packages: Ball Grid Array (BGA) and Fine Pitch Ball Grid Array (FPBGA), Flip Chip Ball Grid Array (FCBGA), Quad Flat-Pack No Leads (QFN), Plastic Quad Flat Back (PQFP)
- HiRel Packages: Hermetic ceramic package technology Ceramic Quad Flat Pack (CQFP), Ceramic Column Grid Array (CCGA), Land Grid Array (LGA), Pin Grid Array (PGA), Dual Flat Pack (DFP)
- QML-V certification per MIL-PRF-38535
- QML-Y (Class Y) facility certification per MIL-PRF-38535 representing the first Class Y certification awarded by the Defense Logistics Agency (DLA)
- QML qualified chip capacitor attach and solder column attach processes

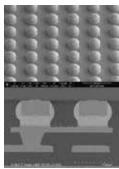
Plug & SenseSM Packaging Examples

- · Flip-Chip on Flex, Organic, or Ceramic assembly
- · Stacked Sensor to ASIC design
- · 4,096 Channel Bio-Sensor with 2 ASICs
- Two 512 Channel Flip-Chip ASICs plus Flip-Chip Bio Sensor

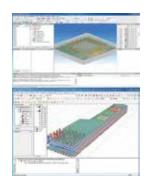
Advanced Package Technology

- QML stacked SRAM memory assembly
- QML MRAM magnetic shielding assembly
- · Advanced Ceramic Flip-Chip assembly (Class Y)
- RF & digital logic integration in 2.1D Multi-Chip Module on Organic Substrates
- Wafer bumping on thin class III-V wafer substrates

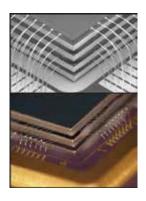












RF Microwave Products

CAES, A Trusted Supplier, has been providing RF Microwave custom products for over 15 years. Our engagement models include build to spec and build to print. Components include amplifiers, attenuators, couplers, mixers, power dividers and switches.

Microwave Module Capabilities

caes.com/HiRel

- Conventional thick/thin film substrate "chip and wire" metal or ceramic packages
- · Analog/Digital circuit design & packaging
- High temp co-fired ceramic (HTCC) and low temp co-fired ceramic (LTCC) packaging
- · Fluxless flip chip attach on ceramic substrate
- RF Microwave GaAs, Si, SiGe, & GaN die attach using DAP vacuum furnace, wire bonding and electrical test
- ASIC Integration linear, digital, and mixed signal in MCM packages
- · Value added surface mount board assemblies
- · RF and microwave module design, fab and test up to 65 GHz
- Stand-off Stitch, Substrate Attach, LTCO, Aluminum Nitride Substrate, Microwave Isolation Techniques

Highly Integrated RF Modules

caes.com/HiRel

- 50 kHz to 15 GHz High Gain Modulator Driver Amplifier
- Component integration on a single board to reduce size, cost and improve performance
- CAES designed & manufactured multilayer thick-film substrate
- · Built in DC Control Circuitry
- Conductive Walls with Solid Vias under Walls to Optimize Ground and Provide Superior Isolation
- Co-planar waveguide thin film for Impedance Matching
- Laser Trimmed Resistors to Facilitate Active Trimming
- Seam Welded Hermetic Construction (10-8)



Features of a CAES L-Band Low Noise Amplifier

caes.com/HiRel

- Input Supply Voltage: +4.9 to +5.1 V_{DC}
- · DC Supply Current: 40 mA
- RF Input Power with internal power limiter: +27dBm CW/Peak
- Baseplate Temperature, Operating & Non-Operating: -55°C to +125°C
- Noise Figure, 0.5dB 1.400 GHz to 1.427 GHz, from -20°C to +40°C
- Noise Figure versus Temperature: 0.01 dB/°C
- Gain: 29 31 dB
- Gain Flatness: 0.1dB from 1.400 GHz to 1.427 MHz
- Gain Matching (Unit to Unit): -0.5dB to 0.5dB from 1.400 GHz to 1.427 GHz
- Gain Variation versus Temperature: 0.015 dB/°C
- Phase Linearity: -5 to +5 Degrees from 1.400 GHz to 1.427 GHz
- Phase Stability vs Temperature: 0.07 Degrees/°C from 1.400 GHz to 1.427 GHz
- Phase Matching (Unit to Unit):
 -5 to +5 Degrees from 1.400 GHz to 1.427 GHz
- Total Output Noise Power:
 - -37dBm from DC to 26GHz when terminated in a 50W input load
- Output Power at 1dB Compression: +7.5dBm from 1.200 GHz to 1.616 GHz
- Input / Output VSWR: 1.5: 1 from 1.400 GHz to 1.427 GHz
- Total Ionizing Dose (TID): 100 krad(Si) with dose rates of 0.005 krad(Si)/sec and 50 rad(Si)/sec
- Single Event Effects (SEE): 37 MeV cm²/mg
- Single Event Latch-Up (SEL): 75 MeV cm²/mg
- Dimensions: 1.72" L X 0.70" W X 0.29" H (43.68 mm x 17.78 mm x 7.36 mm)





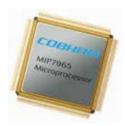
Typical Screening Levels caes.com/HiRel

- Screened & Qualified to the requirements of MIL-PRF-38534 Class K
- Element Evaluation IAW the requirements of MIL-PRF-38534 Class K
- · Additional Screens include Random Vibration

MIPS RISC 64Bit Microprocessors caes.com	Description	CPU Speed (MH	z) Package
ACT-700ASC-300F1700	64 bit SysAD bus interface in a cavity-up hermetic CQFP	300	208 CQFP (1.12" sq)
ACT-700ASC-300F2400	64 bit SysAD bus interface in a cavity-down hermet ic CQFP	300	208 CQFP (1.12" sq)
MIP7365-450B100*	64 bit SysAD bus interface in a TBGA	450	Plastic 256 TBGA (26mm sq)
MIP7965-668F17(X)	64 bit SysAD bus interface in a cavity-up hermetic CWFP with EJTAG debug port	668	208 CQFP (1.12" sq)

* Contact Factory

(X) = Temperature range and screening code (see data sheet)





Memory Modules caes.com

Description

Access Speed (ns)

Package

High-Speed, low-noise, low-voltage TTL (LVTTL) compatible outputs. 3.3V operation with separate logic and output driver power pins. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors. Internal pipelined operation; column address can be changed every clock cycle. CAS latency (CL) programmable to 2 cycles from column-address entry. Cycle-by-cycle DQ-bus write mask capability with upper and lower byte control. Chip select and clock enable for enhanced-system interfacing. Auto-Refresh.

ACT-D1M96S-020F20X Ordering Part Number: 3369-BF20-M01C	6 low power 1M x 16 banks of SDRAM die packaged into a single SDRAM MCM organized as 2 independent 512K x 48 x 2 banks. Programmable burst lengths: 4 or 8. Serial Burst Sequence. 2 banks for on-chip interleaving (gapless accesses). 4K refresh (Total for Both Banks) Operates from 3.3V Power Supply +/-10%.	20	200 CQFP (1.45" sq)
ACT-D16M96S-020F20X Ordering Part Number: 3370-BF20-M21C-1	6 low power 4M x 16 x 4 banks of SDRAM die packaged into a single SDRAM MCM organized as 2 independent 4M x 48 x 4 banks. LVTTL compatible outputs. $3.3V$ operation with separate logic and output driver power pins. Internal pipe-lined operation; column address can be changed every clock cycle. Programmable burst lengths: $1,2,4,8,$ or full page. $64 \text{ms}, 8,192$ -cycle refresh. Autoprecharge, includes concurrent auto precharge, and auto refresh modes. Operates from $3.3V$ power supply $\pm 5\%$.	20	200 CQFP (1.45" sq)

Motor Drivers caes.com	Description	Package
ACT5 101-1 Three Phase Brushless DC Motor Driver	The ACT5101-1 is a three phase, 500V rated, motor driver intended for high power/high reliability trapezoidal and sinusoidal applications. The ACT5101-1 features highly efficient IGBT output transistors capable of delivering 50 Amps of continuous current. Each IGBT is independently driven which enables 4-quadrant motion control and dynamic braking. Self-protection circuitry is employed to eliminate shoot-through events of in-line transistors. IGBT gates are driven with individually isolated floating supplies, not bootstrapping. This configuration allows for the use of sense resistors in any or all legs of the motor. Additionally, the ACT501-1 is capable of supplying continuous stall currents.	26 Plug-in package (3.0" x 2.1" x 0.39"

MIL-STD-1553 Encoder-Decoder caes.com

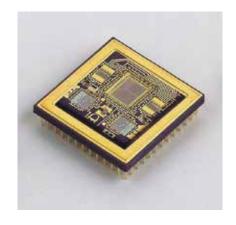
Description



CT1820 Data terminal bit processor for MIL-STD-1553 A & B, +5V 56-pin plug-in 2.2" x 1.2" also available in a 1.0" x 1.7" 60-lead flatpack.

5962-90636

MIL-STD-1553 Integrated Terminals caes.com	Description	%ONS
CT2542 / CT2542-FP	$78\mbox{-pin quad plug-in 1.9"} \times 2.1" \mbox{ or } 82\mbox{-lead flatpack; dual redundant remote terminal with dual transceivers; +5V, -15V; } \\ 16\mbox{-bit bus; } 16\mbox{ MHz; direct replacement for BUS65142}.$	5962-8979803
CT2553 / CT2553-FP	$78-pin \ quad \ plug-in \ 1.9" \ x \ 2.1" \ or \ 82-lead \ flat pack; \ dual \ redundant \ BC/RT/MT \ protocol \ unit \ with \ dual \ transceivers; \ 8K \ x \ 16 \ Ram; +5V, -15V; \ direct \ replacement \ for \ BUS 61553.$	5962-8869201
CT2554 / CT2554-FP	Same as CT2553 except +5V, -12V; direct replacement for BUS61554.	5962-8869202
CT2555 / CT2555-FP	Same as CT2553 except +5V only; direct replacement for BUS61555.	5962-8869203
CT2578-P119	119-pin CPGA 1.3" sq.; Simple RT protocol unit with dual MIL-STD-1553 A/B transceivers; DMA handshake; +5V.	
CT2578-F84	Similar to CT2578-P119 except 84-lead CQFP 1.16" sq.	
ACT7006	Same as ACT7005 except with external SSF status bit control.	



MIL-STD-1553 Databus Transceivers Single Channel caes.com	15537.	160 Moca.		P. 24.88 T. 10.0	, Joe 27		Power Schooles	Tums	Cery Office Constitution	SMO # ONO.
ACT4402			0.62" x 1.25"	Plug-in	24	Low	+5V, ±15V	1.4:1		5962-86049
ACT4402I			0.62" × 1.25"	Plug-in	24	High	+5V, ±15V	1.4:1		
ACT4404N** (replaces CT3232M)		•	1.27" × 1.27"	Plug-in or Flatpack	24	High	+5V, ±12V to ±15V	1:1	Open	5962-91749
ACT4438-1, ACT4438-3			8 mm x 8 mm	BCC++	56	Low	+5V	2.5:1		
ACT4455			0.445" x 0.445"	LCC	28	Low	+5V	2.5:1		5962-96741
ACT4459			0.445" x 0.445"	LCC	28	High	+5V	2.5:1		5962-96741
ACT4406N (replaces ARX3404)	•	•	1.27" × 1.27"	Plug-in or Flatpack	24	High	+5V, ±12V to ±15V	1:1	Open	5962-89592
ACT4407N (replaces CT3231M)			1.27" × 1.27"	Plug-in or Flatpack	24	High	+5V, ±12V to ±15V	1:1	Open	5962-91749
ACT4418N*			1.27" × 1.27"	Plug-in or Flatpack	24	Low	+5V, ±12V to ±15V	1:1	Open	5962-92085
ACT4435N (replaces CT1816 and CT1641)		H009	1.27" × 1.27"	Plug-in or Flatpack	24	High	+5V, ±12V to ±15V	1:1	Open	
ACT4487 (equiv BUS8553) (replaces CT1487 and CT1487M)	•		0.805" x 1.385" 0.735" x 1.315"	Plug-in and Flatpack	24	High	+5V, ±15V	1.4:1	•	
ACT4489				Plug-in and Flatpack	24		+5V, ±12V	1:1		
ACT4467N				Plug-in and Flatpack	24	Low	+5V, ±12V to ±15V	1:1		

 $^{^{\}star}$ Variable Amplitude Transceiver (similar to ARX4418) - contact factory for information. ** Has external threshold control.

MIL-STD-1553 Databus Transceivers Dual Channel* caes.com	1553/1/60 Media	3	P. O.	2697 2697 1746 77	Solitor Solitor	Zamzi Zamzi	Tangon Construction	PUTO DO 4 ONS
ACT4419D		0.3" x 1.2"	Plug-in	20	+5V	2.5:1		
ACT4419DF		0.3" x 1.2"	Flatpack	20	+5V	2.5:1	•	
ACT4453		0.775" x 1.9"	Plug-in or Flatpack	36	+5V	2.12:1	•	5962-89522
ACT4458		0.6" x 0.8"	Flatpack	24	+5V	2.5:1		5962-92061
ACT4464		0.6" x 0.8"	Flatpack	24	+5V	2.5:1		5962-92061
ACT4461DF		0.6" x 0.8"	Flatpack	24	+5V	2.5:1		
ACT4468D (equiv NHI-1567)		0.3" x 1.0"	Plug-in	20	+5V	2.5:1		
ACT4468DF		0.3" x 1.0"	Flatpack	20	+5V	2.5:1		
ACT4462D (pin selectable H009 transmit- ter)	■ H009	0.62" x 1.25"	Plug-in	24	+5V, ±12V to 15V	1:1	Open	
ACT4469D	H009	0.62" x 1.25"	Plug-in	24	+5V, ±15V	1:1		
ACT4479D	H009	0.775" x 1.5"	Plug-in	28	+5V, ±15V	1:1		
ACT4479DF	H009	0.775" x 1.5"	Flatpack	28	+5V, ±15V	1:1		
ACT4480-DFI	H009	0.6" x 0.8"	Flatpack	24	+5V, ±12V to15V	1:1		
ACT4489D		0.775" x 1.9"	Plug-in	36	+5V, ±12V	1:1		
ACT4489DF		0.775" x 1.9"	Flatpack	36	+5V, ±12V	1:1		
ACT4433D		0.775" x 1.5"	Plug-in	28	+5V, ±12V	1:1		
ACT4433DF		0.775" x 1.5"	Flatpack	28	+5V, ±12V	1:1		
ACT4487D (replaces CT1487D)		0.775" x 1.9"	Plug-in	36	+5V, ±15V	1.4:1		5962-87579
ACT4487DI (replaces CT1487DI)	•	0.775" x 1.9"	Plug-in	36	+5V, ±15V	1.4:1		5962-89447
ACT4487DF (replaces CT1487DFP)	•	0.775" x 1.9"	Flatpack	36	+5V, ±15V	1.4:1	•	5962-87579
ACT4487DFI (replaces CT1487DIFP)	-	0.775" × 1.9"	Flatpack	36	+5V, ±15V	1.4:1	•	5962-89447
ACT4436D		0.775" x 1.5"	Plug-in	28	+5V, ±15V	1.4:1		
ACT4436DI		0.775" x 1.5"	Plug-in	28	+5V, ±15V	1.4:1		5962-89447
ACT4436DF		0.775" x 1.5"	Flatpack	28	+5V, ±15V	1.4:1		
ACT4436DFI		0.775" x 1.5"	Flatpack	28	+5V, ±15V	1.4:1		5962-89447
ACT4808N-D		0.775" x 1.9"	Plug-in	36	+5V, ±12V to ±15V	1:1	Open	
ACT4808N-DF		0.775" x 1.9"	Flatpack	36	+5V, ±12V to ±15V	1:1	Open	
ACT4454			Flatpack	24	+5V	2.5:1		5962-92061
ACT4460			Flatpack	24	+5V	2.5:1		5962-92061

^{*} See individual data sheets for receiver output idle low/high.



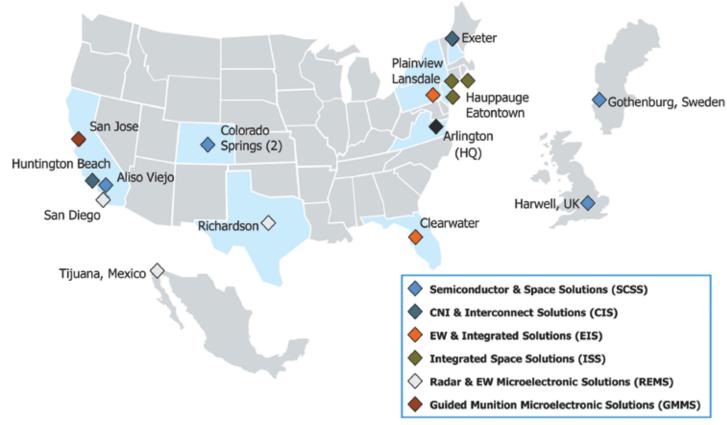


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