

SCD5930

Digital-to-Analog Converter, 11-Bit, Ladder Output

RHD5930

Features

- Radiation performance
 - Total dose: > 1 Mrad(Si); Dose rate = 50-300 rad(Si)/s
 - ELDRS Immune
 - SEL Immune: > 100 MeV-cm²/mg
 - Neutron Displacement Damage: > 10¹⁴ neutrons/cm²
- 11-Bit DAC
- Single power supply operation at +3.3V to +5V
- Low Power
- Full 4-quadrant multiplying DAC
- CMOS/TTL inputs
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic SOIC
 - 16 leads, 0.417"L x 0.300"W x 0.120"Ht
 - Typical Weight 0.8 grams
- **Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.**

General Description

The 11-Bit DAC is a standard CMOS R/2R Kelvin resistor network. The digital inputs, D10_(MSB) through D00(LSB), are buffered to drive single-pole double-throw CMOS switches to apply either the PREF or NREF signals to the 2R legs of the resistor network. The output is unbuffered.

PREF and NREF inputs can be any static or dynamic voltage within the power supply range. The nominal values of R and 2R are 5K and 10K respectively. The characteristic impedance of the resistor network is approximately 5K.

The voltage-output configuration of the integrated circuit can be thought of as a digitally controlled voltage with a value of PREF-NREF and an output impedance of approximately 5K. The output will swing rail-to-rail if unloaded.

The DAC can also be operated in the so-called "inverted" mode where any voltage between the power rails can be applied to the output and currents into a very low impedance (operational amplifier summing junction for example) can be obtained from the PREF and NREF ports. The sum of the currents is constant and the proportion at PREF and NREF is controlled by the digital input number.

Applications include digital potentiometers, programmable voltage sources and a large variety of other circuits that can be found in many industry references.

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Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Lead Temperature (soldering, 10 seconds)	300	°C
Thermal Resistance, Junction to Case, θ_{jc}	7	°C/W
Supply Voltage +V _{CC}	+7.0	V
PREF relative to NREF	+6.0	V
Digital Input Voltage	V _{CC} +0.4 GND -0.4	V
Power @25°C	20	mW

Note:

- 1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Typical	Units
+V _{CC}	Power Supply Voltage	3.3 to 5.0	V

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Electrical Performance Characteristics

(Tc = -55°C to +125°C, +Vcc = +5.0V -- Unless otherwise specified)

Parameter	Symbol	Conditions	MIN	MAX	Units
Supply Current	I _{CC}	Toggle inputs, V _{CC} , GND		1	mA
Quiescent current <u>1/</u>	I _{CCQ}	All inputs = GND		1	mA
Relative Accuracy <u>1/</u>	R _A	PREF = 4.9 V, NREF = 0.1 V		0.25	% of FSR
Gain Error <u>1/</u>	A _E	PREF = 4.9 V, NREF = 0.1 V		0.55	% of FSR
Offset Error <u>1/</u>	O _{FF2}	PREF = 4.9 V, NREF = 0.1 V		0.25	% of FSR
Differential Nonlinearity <u>1/</u>	DNL	PREF = 4.9 V, NREF = 0.1 V		0.25	% of FSR
Output Settling Time	T _D	All inputs = Gnd to V _{CC} , PREF = 4.9 V, NREF = 0.1 V, Output = 1/2 LSB of Nominal		2.75	us
PREF Input Z	Z _P		3	7	KΩ
NREF Input Z	Z _R		3	7	KΩ
Input High Voltage	V _{IH}	PREF = 4.9 V, NREF = 0.1 V	3.5		V
Input Low Voltage	V _{IL}	PREF = 4.9 V, NREF = 0.1 V		1.5	V
Input High Leakage <u>1/ 2/</u>	I _{IH}	Input under test = GND		1	nA
Input Low Leakage <u>1/ 2/</u>	I _{IL}	Input under test = V _{CC}		1	nA
Resolution	N		11		Bits

Notes:

- 1) Specification derated to reflect Total Dose exposure to 1 Mrad(Si) @ +25°C.
- 2) These parameters for Tc = -55°C are guaranteed by design, characterization, or correlation to other test parameters.

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Package Pin #s	Signal	Definitions
1	PREF	Positive Analog Voltage Reference.
2	NREF	Negative Analog Voltage Reference
3	GND	- Voltage Supply
4	D10	Digital Bit 10 (MSB)
5	D09	Digital Bit 09
6	D08	Digital Bit 08
7	D07	Digital Bit 07
8	D06	Digital Bit 06
9	D05	Digital Bit 05
10	D04	Digital Bit 04
11	D03	Digital Bit 03
12	D02	Digital Bit 02
13	D01	Digital Bit 01
14	D00	Digital Bit 00 (LSB)
15	VCC	+ Voltage Supply
16	AOUT	Analog Output

Figure 1: Pinout Descriptions

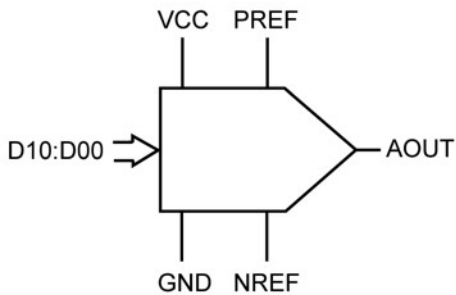


Figure 2: Schematic Symbol

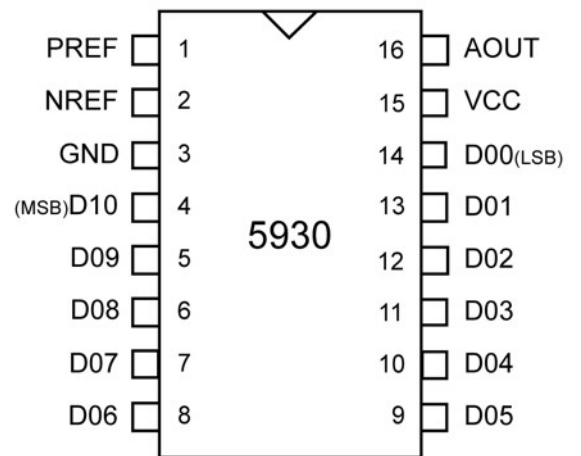


Figure 3: Package Pinout

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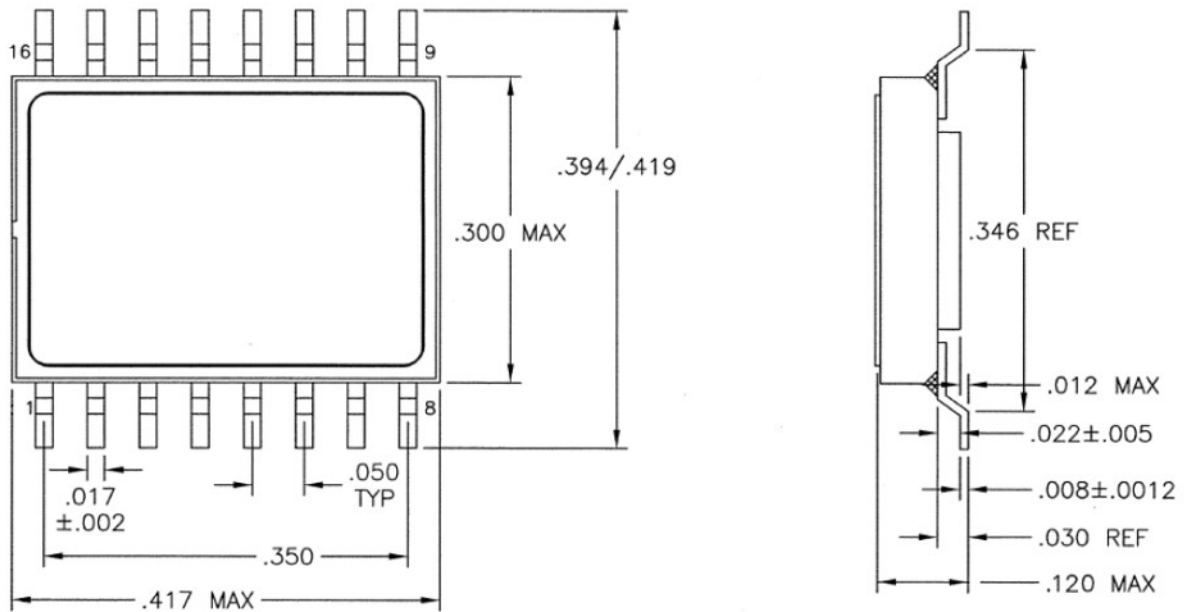


Figure 4: Package Outline

Note:

- 1) Package and lid are electrically isolated from signal pads.

Ordering Information

Model	DLA SMD #	Screening	Package
RHD5930-7	-	Commercial Flow, +25°C testing only	16-pin SOIC Package
RHD5930-S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD5930-201-1S	5962-1120801KXC	In accordance with DLA SMD	
RHD5930-201-2S	5962-1120801KXA		
RHD5930-901-1S	5962H1120801KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "H", 1 Mrad(Si)	
RHD5930-901-2S	5962H1120801KXA		

Revision History

Date	Revision	Change Description
03/28/2016	C	Import into CAES format
03/15/2021	E	Revised per ECN 23555.

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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