PROBLEM ADVISORY

CAES

1. TITLE GRFPU Floating-point controller: Missing FDIV/FSQRT Result	**2. DOCUMENT NUMBER** SPO-2020-PA-0003
	3. DATE *(Year, Month, Date)* 2018, February 22nd

4. MANUFACTURER NAME AND ADDRESS CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486	**5. MANUFACTURER POINT OF CONTACT NAME** Gaisler Support
	6. MANUFACTURER POINT OF CONTACT TELEPHONE +46 (0) 31 775 8650
	7. MANUFACTURER POINT OF CONTACT EMAIL support@gaisler.com

8. CAGE CODE 65342	**9. LDC START** **1836/1507/1535**	**10. LDC END** **1935/1906/1939**	**11. PRODUCT IDENTIFICATION CODE** See table below for PA	**12. BASE PART** See table below
13. BLANK			**14. SMD NUMBER** See table below	**15. DEVICE TYPE DESIGNATOR** 01
			16. RHA LEVELS R	**17. QML LEVEL** See table below
			18. NON QML LEVEL N/A	**19. GIDEP NUMBER** GB4-P-20-03A

20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT

This document describes a corner case present in the GRFPC floating point controller, which is the hardware used to interface the GRFPU floating point unit with the LEON3/FT and LEON4/FT processors. The corner case described in this document can cause a FDIV/FSQRT operation result not to be committed to the floating point register file. The issue manifests if;

- two instructions exist in the instruction flow between two FDIV/FSQRT instructions, and
- at least one of them is a floating point operation, and
- the processor encounters certain number of hold cycles after the first FDIV/FSQRT operation reaches execute stage of the pipeline.

Base part number	PIC	SMD number	QML Level
UT699	WG07	5962-08228	Q,V
UT699E	WQ02	5962-13237	Q
UT700	WQ03	5962-13238	Q,V

GRFPU Floating-point controller: Missing FDIV/FSQRT Result
Technical note 2017-12-21
Doc. No GRLIB-TN-0013
Issue 1.3

21. ACTION TAKEN / PLANNED

Missing FDIV/FSQRT results can be avoided by avoiding the sequence described in section 19.
This can be accomplished by ensuring that at least two instructions exist after an FDIV/FSQRT operation which is not a FPop1 type operation. If not, insert an extra NOP instructions after the FDIV/FSQRT until the vulnerable sequence is avoided.

The compiler workaround will do the following to prevent vulnerable sequences from being
Generated (BCC 1.0.50, BCC 2.0.2, RCC 1.2.22, RCC 1.3-RC3, VxWorks 6.7 1.0.21 – Toolchain 1.0.15,, VxWorks 6.9 2.0.8 – Toolchain 1.0.4, VxWorks 7 – Toolchain 7.2.0.0, and MKPROM 2.0.63). More information on GRLIB-TN-0013, send a request to support@gaisler.com

22. DISPOSITIONARY RECOMM **23. ENDATION:**	CHECK & USE AS IS ☒	CONTACT ☐ MANUFACTURER	REMOVE & ☐ REPLACE	CORRECT & ☐ USE AS SPECIFIED
24. ADEPT REPRESENTATIVE **Lin-Chi Huang**	**25. SIGNATURE**			**26. DATE** 2018, February 22nd